1 General Notes

1.1 Test Equipment

1.1.1 Test Equipment for Repairs and Adjustments (see chapters 4 to 7)

The extent to which the SNA-20/-23 can be serviced depends on the test equipment available. The requirements have been split into 4 (+1) stages. The requirements for repair, replacement of printed circuit boards or adjustment of individual subassemblies are listed in chapter 1.2 on page 1-3.
A general check of the instrument should be made after every repair, pcb replacement or adjustment. A generator covering the same frequency range as the SNA is required for this. Refer to chapter 8 for more details.

Test equipment required

Requirement 1: (basic equipment)	Digital multimeter; 4 1/2 or (preferably) 5 1/2 digits Oscilloscope (400 MHz, with RF probes) Frequency counter
Requirement 2:	Requirement 1 + Selective level meter, level generator (22 MHz, 50 Ω) (e.g. PSM-139 or PS-19/SPM-19 with 2 x ZA 5075) + high-impedance probe (TK-11) + Spectrum and network analyzer, up to 500 MHz (up to 180 MHz in certain cases only) e.g. SNA-62 (SNA-1, SNA-2 or SNA-3 in some cases)
Requirement 3:	Requirement 2 + Spectrum analyzer (30 GHz [22 GHz]) (e.g. SNA-23/-33, SNA-7)
Requirement 4 :	Requirement 3 + Generator (Sweeper) HP 83640A + Power splitter HP 11667B + Power meter HP 838 A + Power sensor HP 8485 A + (10 dB DG HP 8493 C)? + Personal Computer PC AT 486 with national IEEE bus **+ Software SWP-XY (for frequency response correction)** *Note:* Requirement 4 includes the test equipment for measuring the frequency response.
Other items:	PSS-16 EPM-1 30 dB attenuator (2101-6521.002) Frequency standard (10 MHz ± 10^{-9})

1.1.2 Test Equipment for Verifying the Specifications (see chapter 8)

Refer to section 8.2 for details.

1.1.3 Accessories / Adapters

Description	Recommended type / Order no.	Manufacturer
Torque wrench for SMA screw connectors on microwave subassemblies	0000-7689.262	Suhner/W&G
Adapter cable (50-way ribbon cable), link between interface board and measurement unit controller		W&G
Adapter cable (34-way ribbon cable), link between interface board and measurement unit controller		W&G
2 x BNC to MCX plug adapter cables	2112-6546.003	W&G
BNC to MCX socket adapter cable	2112-6506.014	W&G
Adapter board for adjustment of logarithmizer	Test board 34-2101	W&G
External AT keyboard (MF-2 compatible)	Cherry G80 -1000 or similar	Cherry

1.1.4 Service Disk

Programs on the service disk

The service disk contains the following programs:

Program name	Use
- EEPROM	For initializing the EEPROM check sums for pcbs where the hardware status is stored in an EEPROM on the pcb itself.
- Form_B	For formatting the RAM disk on the memory board.

Using the service disk

The service disk is a boot disk, i.e. the operating system (DOS) can be loaded from the disk. If these programs are to be used, please note the following:

- Place the service disk in drive A:\ of the SNA and then switch the SNA on. This ensures that the operating system is loaded from the disk and the instrument (measurement) software is not loaded.
- If you want to change from one service program to another, first switch off the instrument and then reboot it from the disk.
- Batch files with the "names" of the service programs are located in the root directory of the disk. These batch files should always be used to start the service programs, as other files in addition to the *.EXE files are required for running the programs. The batch files load these automatically.

Important: The service disk programs may also be used for development purposes in addition to their service functions. Incorrect entries are normally not intercepted by the program, and the plausibility of entries is not checked. These programs do not conform to the general standards of quality which apply to Wandel & Goltermann software products.

1.2 Service Scope and Test Equipment Requirements

1.2.1 Servicing the Input Section Subassemblies

Circuit board or sub-assembly	Name	Service action	Test equipment requirement (adjustments required)
2 P38	RF converter (Rosenberger)	Subassembly replacement	Requirement 4 (Frequency response correction)
2 AT1	Attenuator	Subassembly replacement	Requirement 4 (Frequency response correction)
2 FL1	8 GHz lowpass (Suhner)	Subassembly replacement	Requirement 4 (Frequency response correction, input section level correction)
2 K1 2101-ZH (2 DX1)	Coaxial relay (Series A+ B) Diplexer (from series C, replaces coaxial relay 2K1)	Subassembly replacement	Requirement 4 (Frequency response correction, input section level correction)
2101-ZA	Integration Band 0, complete (Series A to E)	Subassembly replacement	Requirement 4 (Frequency response correction, input section level correction)
2101-ZC	Fundamental mixer, complete	Subassembly replacement	Requirement 4 (Frequency response correction, input section level correction)
2101-ZE incl. 2101-AQ	IF switch, complete	Subassembly replacement	Requirement 4 (Frequency response correction, input section level correction)
2101-AS1 plus 3FI1	**Service kit** YIG filter control plus YIG filter (YIG filter calibrated and matched with control unit. The YIG correction data are stored in FLASH EPROMS on the control unit)	Subassembly replacement	Requirement 4 (Frequency response correction)
2101-AR	Input section control	Repair/Subassembly replacement	Requirement 1 (External mixer bias)

The test equipment for each requirement category is listed in section 1.1.1 on page 1-1

1.2.2 Servicing the Synthesizer Subassemblies

Circuit board or sub-assembly	Name	Service action	Test equipment requirement (adjustments required)
2101-B	Time-base / YTO driver	Repair/Sub-assembly replacement	Requirement 1 + Spectrum analyzer up to 9 GHz (Requirement 3) (YTO frequency limits / switching noise)
2101-F	400 MHz oscillator	Repair/ Subassembly replacement	Requirement 1 (LC resonance adjustment)
2101-C	Standard frequency adapter (NFO adapter)	Repair/ Subassembly replacement	Requirement 1 + frequency standard (10 MHz std. freq. adjustment)
50 OS1	(YTO) YIG oscillator (Sievers)	Subassembly replacement	Requirement 4 (YTO frequency limits, frequency response correction)
2101-A	Synthesizer control	Subassembly replacement	Requirement 1 (no adjustment)
2101-ZG	SHF pre-attenuator	Subassembly replacement	Requirement 1 (no adjustment)
2101-K	Synchronous attenuator / phase meter	Subassembly replacement	Requirement 1 (no adjustment)

The test equipment for each requirement category is listed in section 1.1.1 on page 1-1

1.2.3 Servicing the 422 MHz/10 kHz Converter and the IF Measurement Section Subassemblies

Circuit board or sub-assembly	Name	Service action	Test equipment requirement (adjustments required)
6 IF-1	422 MHz bandpass (Interdigital filter)	Subassembly replacement	Requirement 2 (Input section level correction)
2101-X	422/22 MHz converter	Subassembly replacement	Requirement 2 (Input section level correction)
2101-Y	422 MHz/10 kHz converter	Subassembly replacement	Requirement 2 (Input section level correction)
IF selection, complete 2101-L plus 5 x 2101-R 5 x 2101-S	**Service kit** IF selection incl. 5 x LC bandpass and 5 x amplifier stage	Repair/ Subassembly replacement	Requirement 2 + PSS-16 (IF selection adjustment)
Logarithmizer, complete 2101-M plus 10 x 2101-Q	**Service kit** Logarithmizer incl. 10 x 10 dB log. stages (The correction data for the logarithmizer are stored on disk.)	Subassembly replacement	Requirement 2 (Installation of logarithmizer correction data)
2101-O	**Service kit** IF converter (Matched subassemblies)	Subassembly replacement	Requirement 1 (no adjustment)
2101-P	Measurement section control	Subassembly replacement	Requirement 1 (no adjustment)
2101-N	Calibration generator	Repair/ Subassembly replacement	Requirement 2 + PSS-16 + EPM-1 + 30 dB DG (2101-6521.002) (or precision power meter, -30 dBm instead of EPM-1, DG and PSS) (Internal and external CAL source level correction) (Demodulator adjustment)

The test equipment for each requirement category is listed in section 1.1.1 on page 1-1

1.2.4 Servicing the Controller Subassemblies

Circuit board or sub-assembly	Name	Service action	Test equipment requirement (adjustments required)
(18) AT 386	AT-CPU (3011-9305.006)	Subassembly replacement	Requirement 1 (Initialize setup) (Initialize hardware code)
4111-A	Screen controller board (BSK-3)	Subassembly replacement	Requirement 1 (Initialize hardware code)
(16) DS 1	Electroluminescent display	Subassembly replacement	Requirement 1 (no adjustment)
2101-AO	Connector board	Repair/ Subassembly replacement	Requirement 1 (no adjustment)
2101-AG	Interface board	Subassembly replacement	Requirement 1 (Initialize hardware code)
2101-AF	Memory board	Subassembly replacement	Requirement 1 (Load software) (Load compensation data) (Initialize hardware code)
2101-AL	Keyboard controller	Repair/Subassembly replacement	Requirement 1 (Initialize hardware code)
2101-AJ	Input keyboard	Repair/Subassembly replacement	Requirement 1 (no adjustment)
2101-AK	Rotary control	Repair/Subassembly replacement	Requirement 1 (Offset)
(18) A1	Floppy disk drive	Subassembly replacement	(no adjustment)

The test equipment for each requirement category is listed in section 1.1.1 on page 1-1

1.2.5 Servicing the Power Supply Unit Subassemblies

Circuit board or sub-assembly	Name	Service action	Test equipment requirement (adjustments required)
CG44 (Gossen)	AC power supply	Subassembly replacement	Requirement 1 (Adjust power supply output voltages)
2101-BD	Voltage distributor	Repair/Subassembly replacement	Requirement 1 (Overtemperature cutout)
2101-BE	24 / 12 V converter	Repair/Subassembly replacement	Requirement 1 (no adjustment)

The test equipment for each requirement category is listed in section 1.1.1 on page 1-1

2 Important Notes

2.1 Safety Instructions

2.1.1 Preventing Electrical Accidents

Safety class

This instrument belongs to safety class I as defined by IEC publication 348 and VDE 0411. The AC line connector shall not be inserted into AC outlets without a protective ground contact, except in specially certified areas.

Checks before repairs and maintenance

Checking the instrument construction

No changes in instrument construction which reduce safety may be made.

Checking the protective ground

Check the connection and general condition by visual inspection and measure the resistance between the protective ground contact and the AC line plug and the instrument enclosure. The resistance must be < 0.1 Ω. Shake the cable during the measurement. Resistance variations mean that the cable is faulty.

Checking the insulation resistance

Measure the insulation resistance between the AC line terminals which have been shorted together and the protective conductor terminal of the instrument using a 500 V insulation tester. Ensure that the instrument's AC line switch is in the ON position. The insulation resistance must be > 2 MΩ.

Opening the instrument

When covers are removed, or parts are extracted with tools, live components may be exposed. Even contact points may be live.

Therefore, before opening the instrument, disconnect all voltage sources.

If it is absolutely essential to carry out calibration, maintenance or repairs while the instrument is opened and connected to a voltage supply, these procedures may only be carried out by a competent technician who is aware of the associated risks.

Capacitors in the instrument may still be charged; consult the circuit diagrams.

Fuses

Only specified fuses shall be used.

Repairs, replacing components

Repairs must be carried out by a competent technician. No changes in the instrument construction, which reduce its safety shall be made. In particular, this applies to creepage paths and component spacing.

Always use original spare parts whenever possible. Other spare parts may only be used if the safety specifications of the instrument are not reduced.

Checks after repairs and maintenance

Check the connection and general condition by visual inspection and measure the resistance between the protective ground contact at the AC line plug and the instrument enclosure. The resistance must be < 0.1 Ω. Shake the cable during the measurement. Resistance variations mean that the cable is faulty.

Insulation resistance

Measure the insulation resistance between the AC line terminals which have been shorted together and the protective conductor terminal of the instrument using a 500 V DC insulation tester. Ensure that the instrument's AC line switch is in the ON position. The insulation resistance must be > 2 MΩ.

2.2 Anti-static Measures

Electrostatic charges and fields may damage or destroy semiconductor components.

It is, therefore, essential to protect all semiconductor components in the instrument from electrostatic charges and fields.

When the instrument is in its enclosure, there are no problems. When the instrument is opened, the DIN 40 021 warning symbol on

- boards and
- assemblies

that are sensitive to STATIC reminds you that special protective measures have to be taken.

warning symbol according to DIN 40 021

Special measures

Grounded person

Only grounded persons using an anti-static workstation shall work on the instrument.

Grounded bracelet

A grounded bracelet is used to earth technicians working at anti-static workstations.

Conducting work surface

The STATIC workstation comprises a conducting work surface with terminals for the bracelet and ground cable.

Ground cable

The ground cable is connected to ground potential. The following reference points provide ground potential:

- the instrument ground connector,
- the protective ground connector,
- other points at ground potential.

Soldering station

The soldering station must be connected to ground. The soldering station must be specially designed for semiconductor components that are sensitive to static (zero-voltage circuit, grounded soldering iron bit).

Spare parts

Until they are needed, components that are sensitive to static should be left in their protective packaging.

They should only be removed from their protective packaging by a grounded person at an anti-static workstation.

2.3 Handling Microwave Subassemblies

Special test equipment and tools are used during production and repair of the microwave subassemblies. For example, the contacts on the ceramic substrate in the microwave subassemblies are made using bonded wires. The semiconductor components used are extremely sensitive to electrostatic charges. For this reason, no components in the microwave circuits should be removed, nor should the power supply (control) board fitted to some modules be removed. Opening these modules will likely result in irreparable damage.

If a fault is present in a microwave module, the module should be replaced completely.

> ***Caution!***
>
> Opening the microwave modules invalidates the guarantee and repair of the modules in the factory is no longer possible.

Handling the microwave step attenuator line

The attenuator (ATTN) is assembled in a clean-room, since even very fine dust particles can adversely affect its performance. Repairs should therefore also be carried out only in a clean-room. Opening the attenuator invalidates the guarantee and repair of the attenuator in the factory is no longer possible.

Handling waveguide lines

When removing waveguide lines, the screw connectors at both ends of the line must always be undone to ensure that the SMA plugs and sockets and the waveguide itself are not subjected to mehanical stress. Under no circumstances should the waveguides be bent.

> ***Important:*** The coaxial SMA screw connectors on the microwave modules and waveguides must be tightened to the prescribed torque value. The torque wrench specified in chapter 1.3 should be used for this.

2.4 Repair of Circuit Boards Fitted with SMD Components

2.4.1 Introduction

To ensure maximum reliability after repair, particular care and attention are required when working on circuit boards fitted with SMDs[1]. Particular attention should be paid to the method used and the required tools and equipment.

Only persons familiar with SMT[1] should carry out such work.
The following rules should be observed:

a) Use the described test technique for SMDs (see chapter 2.4.2 on page 2-5)

b) Observe the SMD repair guidelines (see chapter 2.4.3 on page 2-6).

c) Use only the described SMT soldering and repair methods (see chapter 2.4.4 on page 2-6).

Important: If these guidelines are not followed, it is likely that the component or circuit board will be destroyed or damaged. If it is not possible to fulfil the requirements given, it is better to replace the entire board rather than attempt to repair it.

2.4.2 Test Techniques for SMD Boards

Never make direct connections (e.g. with a probe) to SMDs when you are checking them out. Instead, use tracks, test pads or vias.

If you are using a special probe with a sprung prod, only make contact at the foot of the component (see figure 2-1).

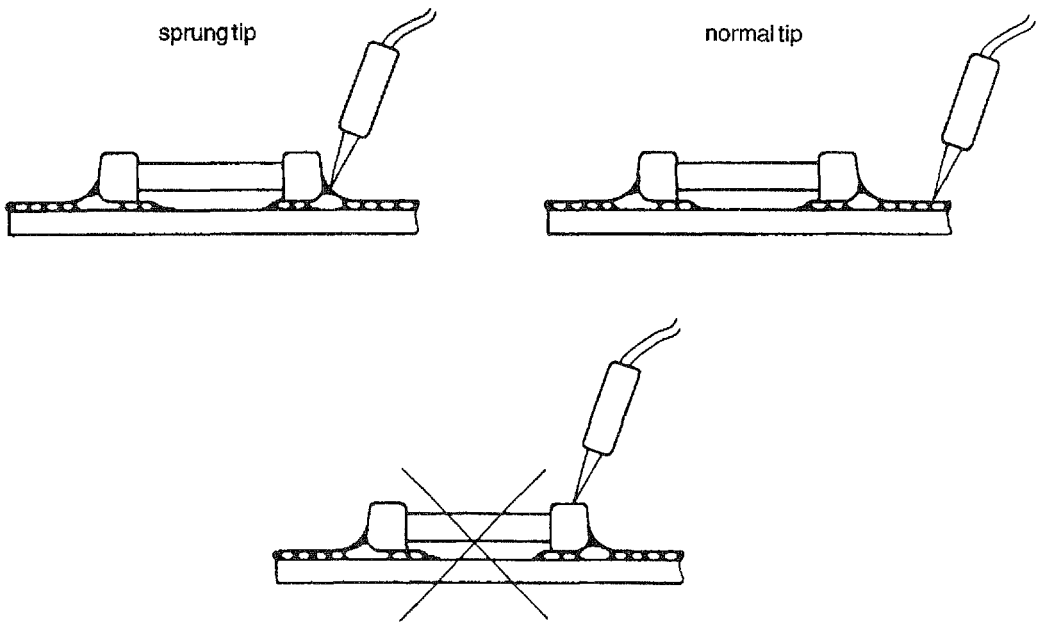


Fig. 2-1 Making measurements on SMD boards

1 Note:
SMD = Surface Mounted Device
SMT = Surface Mounted Technology

2.4.3 Repair Guidelines for Boards with SMDs

If SMDs are handled incorrectly, their properties may be adversely affected. Particular care should therefore be taken. For example, even minimal dirt or impurities on the SMD contacts (e.g. a fingerprint) will prevent wetting during soldering and result in dry joints. The spaces between contacts are often so small that short-circuits are easily caused by solder tracks between them due to the use of unsuitable tools.

The following rules should therefore be observed:

- Only use tools and equipment specially designed for SMD.
- Preferably use special SMD tweezers.
- Do not modify the SMD in any way (use as supplied).
- Keep the SMD in its original packaging until required (the values are not marked on the components!).
- Never hold SMDs with your bare hands.
- Never touch the contacts of SMD with anything other than the special tools (tweezers, clips) intended for this purpose.
- If an SMD is dropped, it should be thrown away (hair-line cracks are likely, particularly in larger components).
- Use only special test tweezers, etc., for checking the value (R or C, etc.) or identity of SMDs which are not mounted on a board.

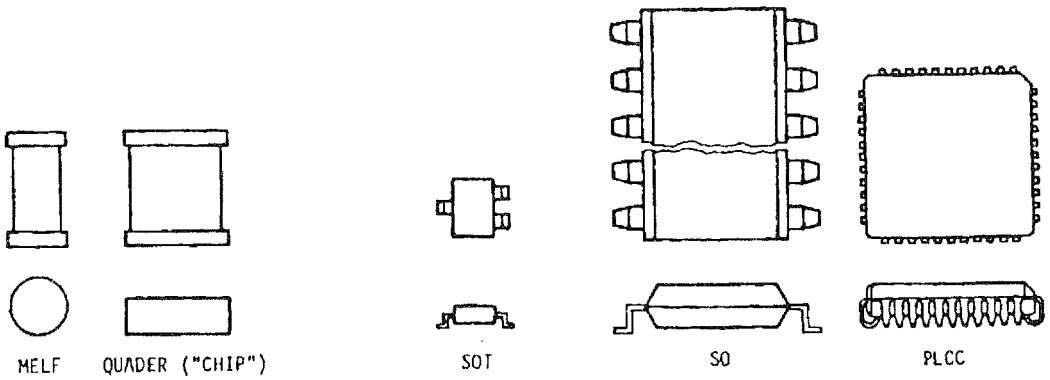


Fig. 2-2 Various SMD outlines

2.4.4 SMT Soldering and Repair Procedures

The object of these procedures is to eliminate soldering faults or to replace defective SMDs. Board faults are eliminated using conventional methods.

When you repair an SMD board, there is a considerably greater risk that components or the board will be damaged. The second eventuality is particularly important because if, say, soldering pads are torn off, it is impossible to mount any SMD without using special adhesive techniques. The board would, therefore, have to be thrown away (see under "Repairing torn-off soldering pads").

Observe the following special SMT rules when carrying out work of this kind

- Soldering iron temperature (bit) = 290 °C (max. 300 °C)
- Maximum temperature of hot gas equipment is 400 °C
- Maximum soldering time 3 s (time for which the solder liquefies)
- Only attempt to repair an SMD once; i.e. do not resolder SMDs which have been unsoldered by mistake, always replace them
- Flux may be used
- Solder paste may be used
- Wire solder may be used

Unsoldering SMDs

- SMDs without pins (Melf + chip) (see Figure 2-2)
  Unsoldering is carried out with hot gas or soldering tweezers. When the component has been removed, the pads must be sucked clear with a desoldering station (fine bit) or a hand desolderer.
- SMDs with a small number of pins (less than 6 pins, SOT, etc.).
- Hot gas is used or the pins can be cut through as with multi-pin ICs.
- SMDs with many pins (more than 6 pins, SO, PLCC)
  Hot gas is used. A simple hot gas station with small hot air jets is not sufficient. It is only possible to remove ICs of this kind, without damaging the board, by using expensive equipment which heats up all the pins at the same time. If you do not have soldering equipment of this type, cut through the pins directly at the component using a cutter, unsolder the pins in the board and suck the solder from the pads.

Soldering SMDs into position

- SMDs without pins
  Use hot gas. The solder must be flowing on both pads simultaneously.
- SMDs with pins
  Use a miniature soldering iron or hot gas. Diagonally opposite IC pins must be soldered alternately.
- Check the joint with a magnifying glass (see Figure 2-3) for bridging, dry joints, cracks and holes, the soldering surface (smooth and evenly shiny), solder drops, splashes and the correct positioning of the SMD.

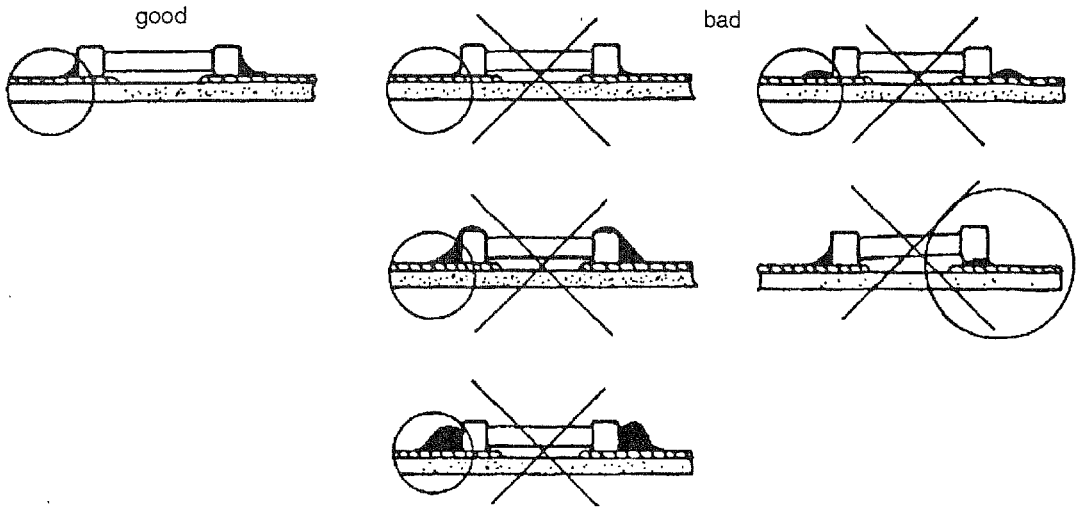


Fig. 2-3 Examples showing soldered SMDs

Repairing torn-off soldering pads

If a soldering pad for an SMD component with pins (IC, PLCC, SOT etc.) has been torn off, solder the component to the board following the usual guidelines and repair the defective pad in the following way:

A varnished wire (d = 0.2 mm) is connected from the component pin to a place of contact near the pad. It is best to use a via. If this is not possible, the wire can be soldered to a soldering pad (as large as possible) of an SMD component.

In the case of SMDs without pins (mini melf / melf resistors, diodes tantalum/multi-layer capacitors, chip resistors, C trimmers, etc.), measures must be taken to ensure the mechanical stability of the soldered joint if a soldering pad is missing.

1 Solder one side of the component to a soldering pad. Connect the other side to a via or an SMD soldering pad which should be as large as possible with a wire (d = 0.6 mm, if necessary insulated). The wire should not be longer than 10 mm.
2 If the method of repair described in 1. cannot be used, the component is held in place with an adhesive.
   - Dot the adhesive on the board.
   - Place component on board.
   - Cure adhesive (100 °C, 20 min).
   - Solder wire (varnished, 0.2 mm) to SMD pin and connect to suitable contact point.

If there is no suitable contact point near the repair, or it is essential to use connections of minimum length, any wide tracks can be used or the solder resist and the black oxide can be scratched from any convenient area and the wire soldered to it.

Recommended solder: wire solder, SnPb 63 d = 0.6 mm or d = 0.3 mm with FSW-32 flux.

2.5 Cleaning the Front Panel and Casing

Never use organic solvents or proprietary cleaning fluids for cleaning the front panel and casing.

The best cleaning fluid is warm water to which a drop of detergent has been added. Use this to slightly dampen a clean cloth. Make sure that no water enters the instrument. To ensure that drying marks are not present, wipe the instrument with a dry cloth after cleaning it.

3 Mechanical Construction

3.1 Instrument Codes

The following instrument codes should be stated when you make enquiries about the instrument or order spare parts:

Type designation, serial number, special version designation, software version number and fitted options.

e.g.: RFS-1, series C-123, BN 2112/03, software (master) V 04.01

When ordering spare parts, the item number given in the parts list in the Annex must also be stated.

e.g.: 1 transistor BCY 59 D, item no.:0001-0016.518

The serial number will be found on the front panel below "RFS-1".

The version number is on the back panel.

3.1.1 Determining the Hardware and Software Status

The hardware and software status of the SNA can be displayed on the screen using the MODE/ CONFIGURATION menu. The hardware and software status must be quoted in all queries regarding the instrument. The menus for displaying the hardware and software status are shown in figure 3-1 and figure 3-2.

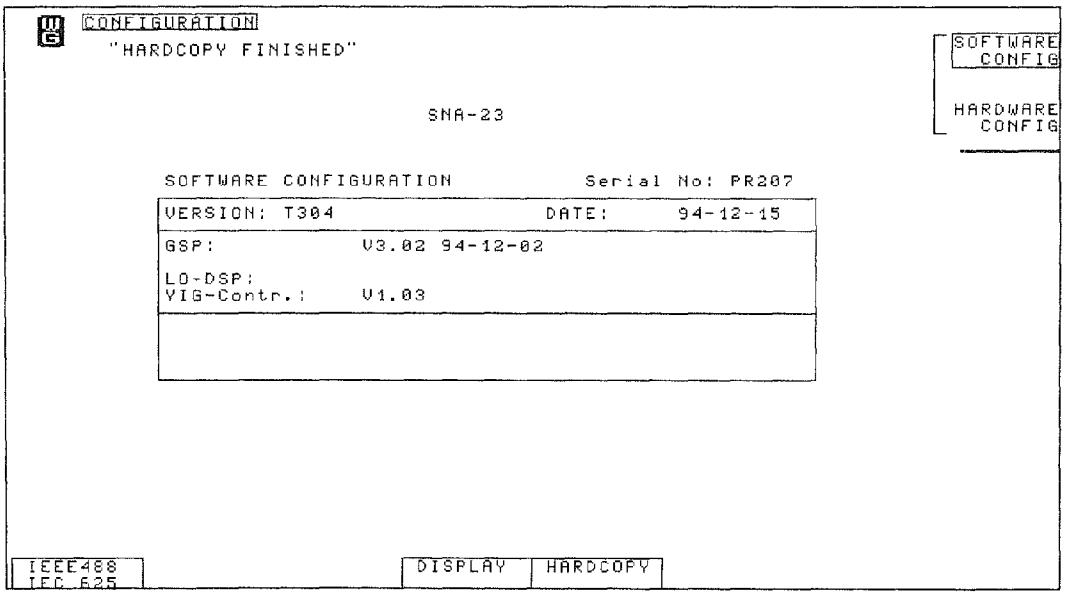


Fig. 3-1 Menu for displaying SNA software status (Example: SNA-23)

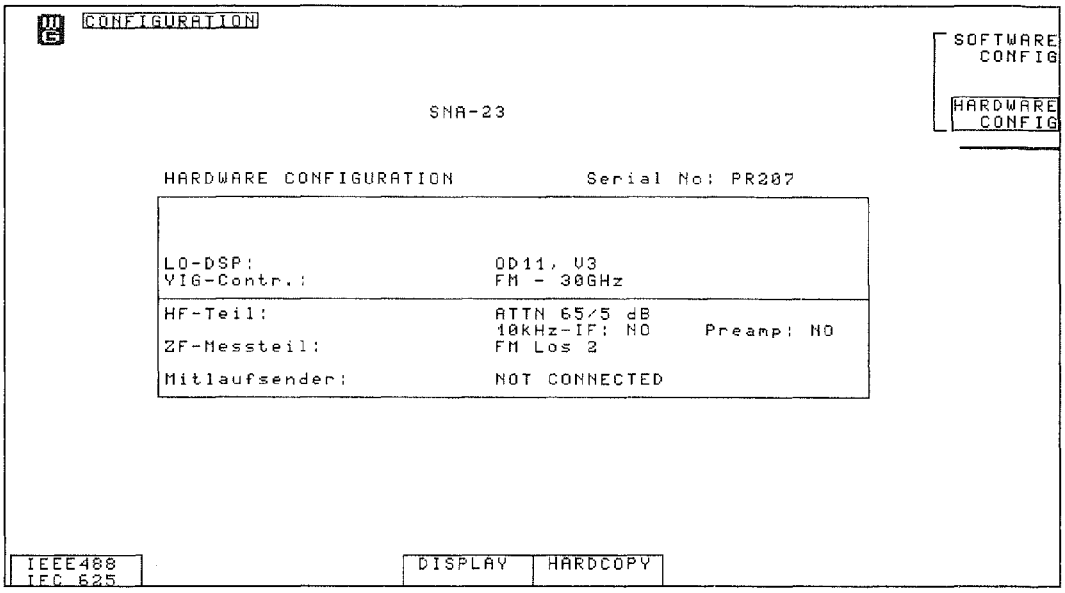


Fig. 3-2 Menu for displaying SNA hardware status (Example: SNA-23)

Some hardware errors may make it impossible to display the software and hardware status of the instrument using the menu, e.g. when the instrument software crashes directly after starting (2101 Debug Output appears in the display). In such cases, the software status can be determined by displaying the files B:\123Time and C:\123Time. C:\123Time contains the information for the instrument software status (AT-CPU and BSK-3 graphics software). B:\123Time contains the information regarding the "layout" of the correction data tables contained on the COMPENSATION DATA DISK and which are copied in the SRAM of the memory board (17).
When the DOS prompt is displayed on the screen, the file contents can be displayed by selecting the drive (B:\ or C:\) and then entering <Type 123Time> (using an external keyboard). This will only work if the AT-CPU is working correctly and drives B:\ and C:\ (board (17), Memory) can be accessed properly. Example displays of these files are shown in figure 3-3 and figure 3-4.

```
GSPV:     3.02          [Graphics software version]
GSPD:     94-12-02      [Graphics software date]
ATV:      T304          [Instrument software version (AT-CPU)]
ATD:      94-12-15      [Instrument software date (AT-CPU)]
```

Fig. 3-3 Display of C:\123Time (example)

```
94-05-11

released: 94-05-11 (2.5)
released: 94-04-22 (2.4)
released: 94-03-28 (2.2)
```

Fig. 3-4 Display of B:\123Time (example)

3.2 Assembly/Disassembly Instructions

3.2.1 Disassembling the Instrument Chassis

Removing the casing cover

To remove the casing cover, unscrew the six hex-key (allen) screws (M4, SW3). Then push back and remove the two impact protector corner pieces. The casing cover can now be removed carefully.

Removing the chassis from the casing

Remove the casing cover as described above and place the instrument top side down on the workbench. Carefully lift the casing off the chassis.

> ***Caution!***
> Make sure that the input sockets and rotary control of the instrument are not subjected to strain. Never hold or lift the instrument using these parts, as damage is likely to result.

3.2.2 Opening the Fold-Out Chassis

The instrument chassis folds out for servicing and maintenance. This provides access to all circuit parts.
Before opening the chassis, remove the instrument from the casing (see chapter 3.2.1).
To open the fold-out chassis, loosen the two knurled screws (between the power supply/voltage distribution board and the fold-out chassis) and undo the two crosshead screws (M3; on the right-hand side of the instrument). These screws are indicated by "A" in the diagram (see figure 3-5 on page 3-4). The chassis can now be folded out completely. The strut on the right-hand side of the instrument can be used to lock the fold-out chassis in the open position for servicing.

The fold-out chassis can be divided into three separate chassis plates by removing a further eight crosshead screws (4 screws on each side of the chassis). Only the screws on the right-hand side of the instrument are shown in figure 3-5 (marked "B").

> ***Caution!***
> When reassembling the fold-out chassis, make sure that the original screws or screws of exactly the same length are used. ***Longer screws will likely result in a short circuit!***

Service position

The instrument can be operated with the chassis folded out when placed normally on the workbench. It can also be operated when placed on its right-hand side with the chassis folded out. It should not be operated for any length of time when placed on its left-hand side (power supply side), as the flow of air to the power supply is hindered: the power supply may overheat and the instrument may switch off automatically.

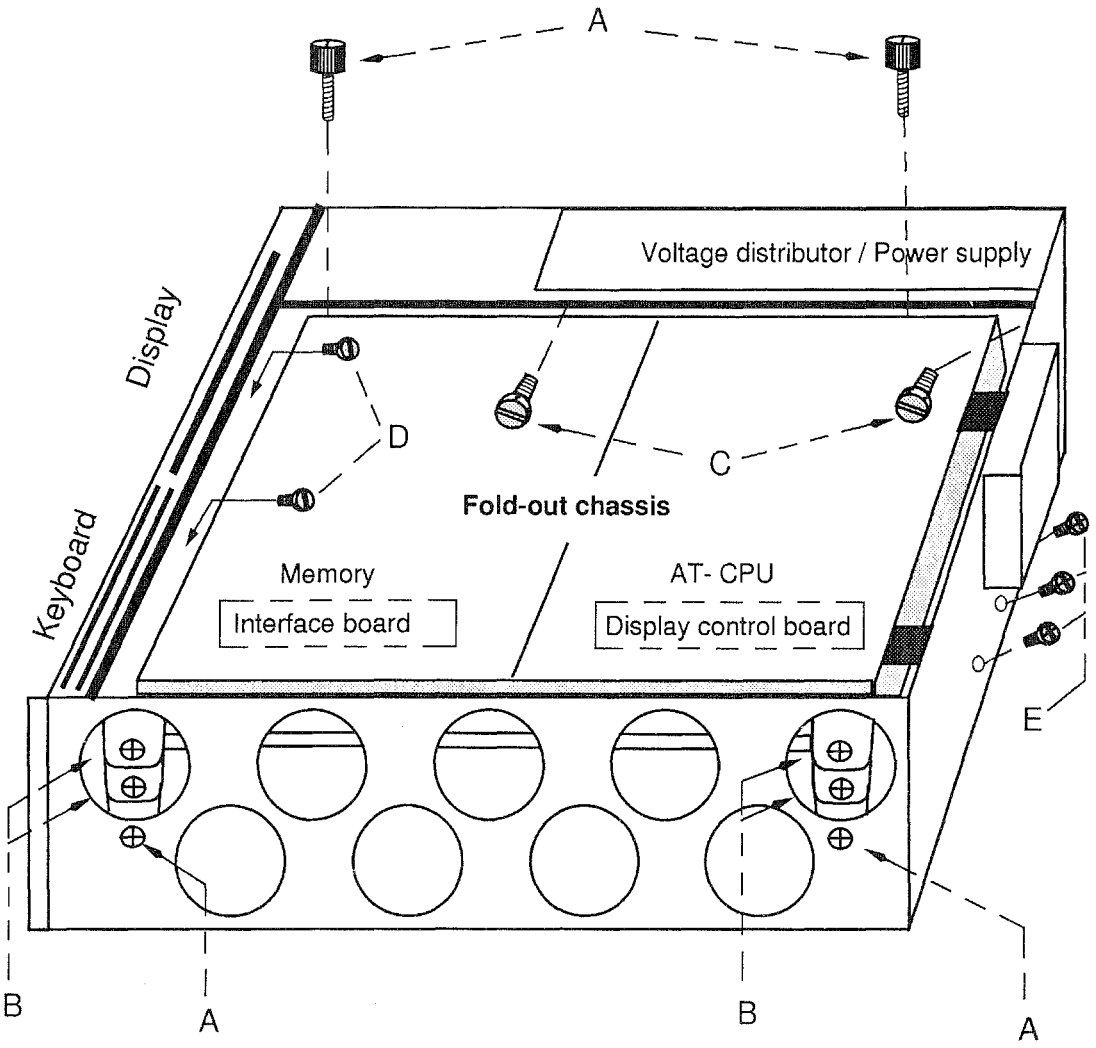


Fig. 3-5 Diagram of instrument showing screws securing the fold-out chassis and the power supply and synthesizer modules (fold-out chassis screening cover removed).

3.2.3 Positions of the Subassemblies

List of boards

Name	Code	For location, refer to
Synthesizer control	2101-A	page 13
Time base/YTO driver	2101-B	page 11
400 MHz VCO	2101-F	page 11
Sync. divider/phase meter	2101-K	page 13
IF selection	2101-L	page 9
Logarithmizer	2101-M	page 9
Calibration generator	2101-N	page 8
IF converter	2101-O	page 8
Measurement module control	2101-P	page 8
10 dB log stage	2101-Q	page 9
LC bandpass	2101-R	page 9
Preamplifier stages	2101-S	page 9
422/22 MHz converter	2101-X	page 10
422 MHz/10 kHz converter	2101-Y	page 10
422 MHz bandpass	IF-1	page 10
Memory board	2101-AF	page 7
Interface board	2101-AG	page 7
Input keypad	2101-AJ	page 7
Rotary control	2101-AK	page 11
Keyboard controller	2101-AL	page 11
Connector board	2101-AO	page 8
Input module control	2101-AR	page 13
YIG filter control	2101-AS1	page 13
12/24 V converter	2101-BE	page 8
Voltage distribution	2101-BD	page 7
Power supply	CG-44	page 7
NFO adapter	2101-C	page 11
Display control board (BSK-3)	4111-A	page 7
Integration band 0	2101-ZA	page 12
Integration band 0 control	2101-CF	page 12
Fundamental mixer	2101-ZC	page 12
Fundamental mixer control	2101-AV1	page 12
IF change-over switch	2101-ZE	page 12
10 MHz crystal oscillator	50 OS101	page 13
Coaxial relay	2K1	page 13
YIG filter	3 FL1	page 13
SHF pre-scaler	2101-ZG	page 13

The current designations (index) are found in the parts list in the Annex to the Service Manual. (Section "Parts Lists")

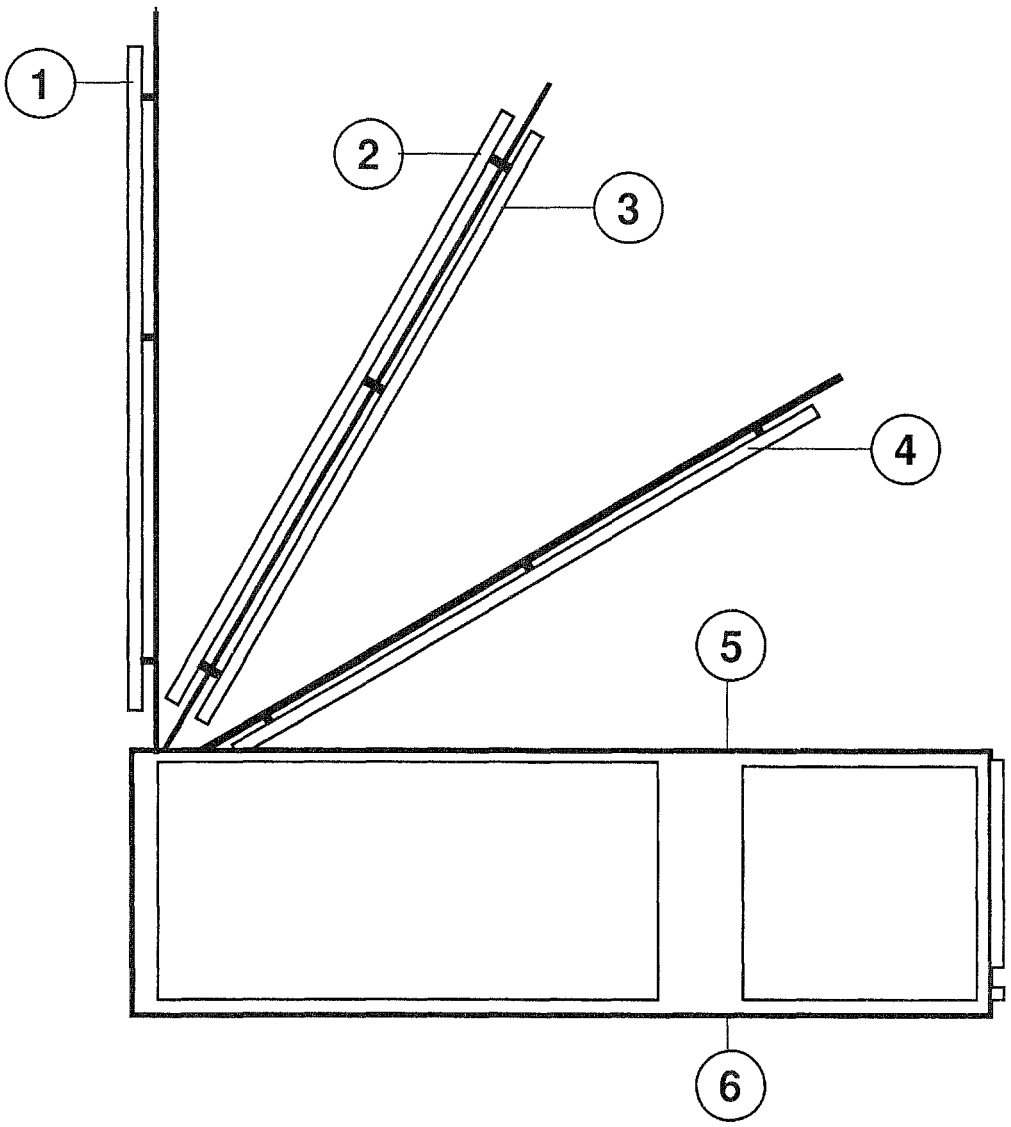


Fig. 3-6 Side view with chassis open

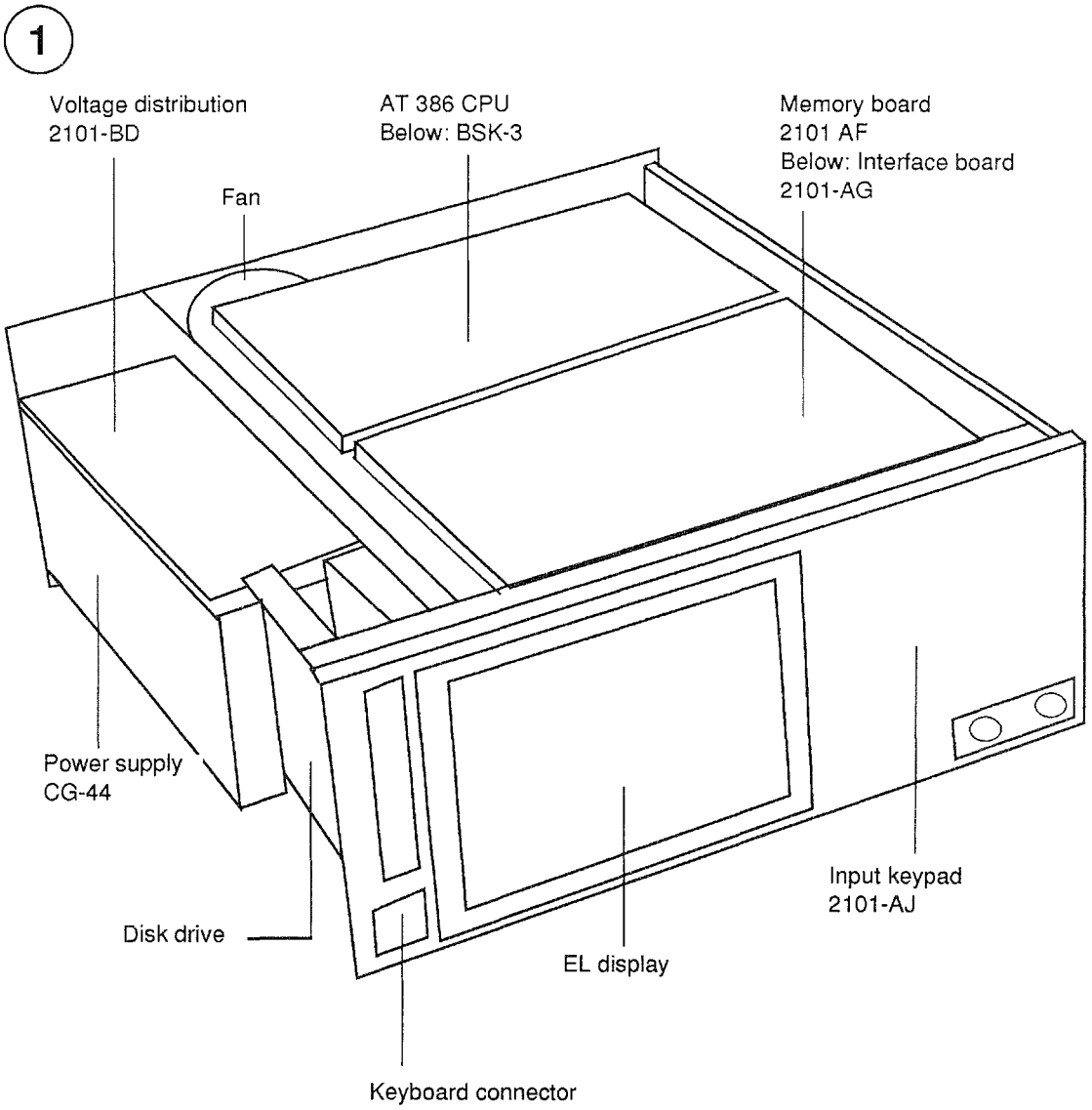


Fig. 3-7 Module positions: AT 386 CPU, Memory board, BSL Interface board, PSU distribution, PSU and Input keypad

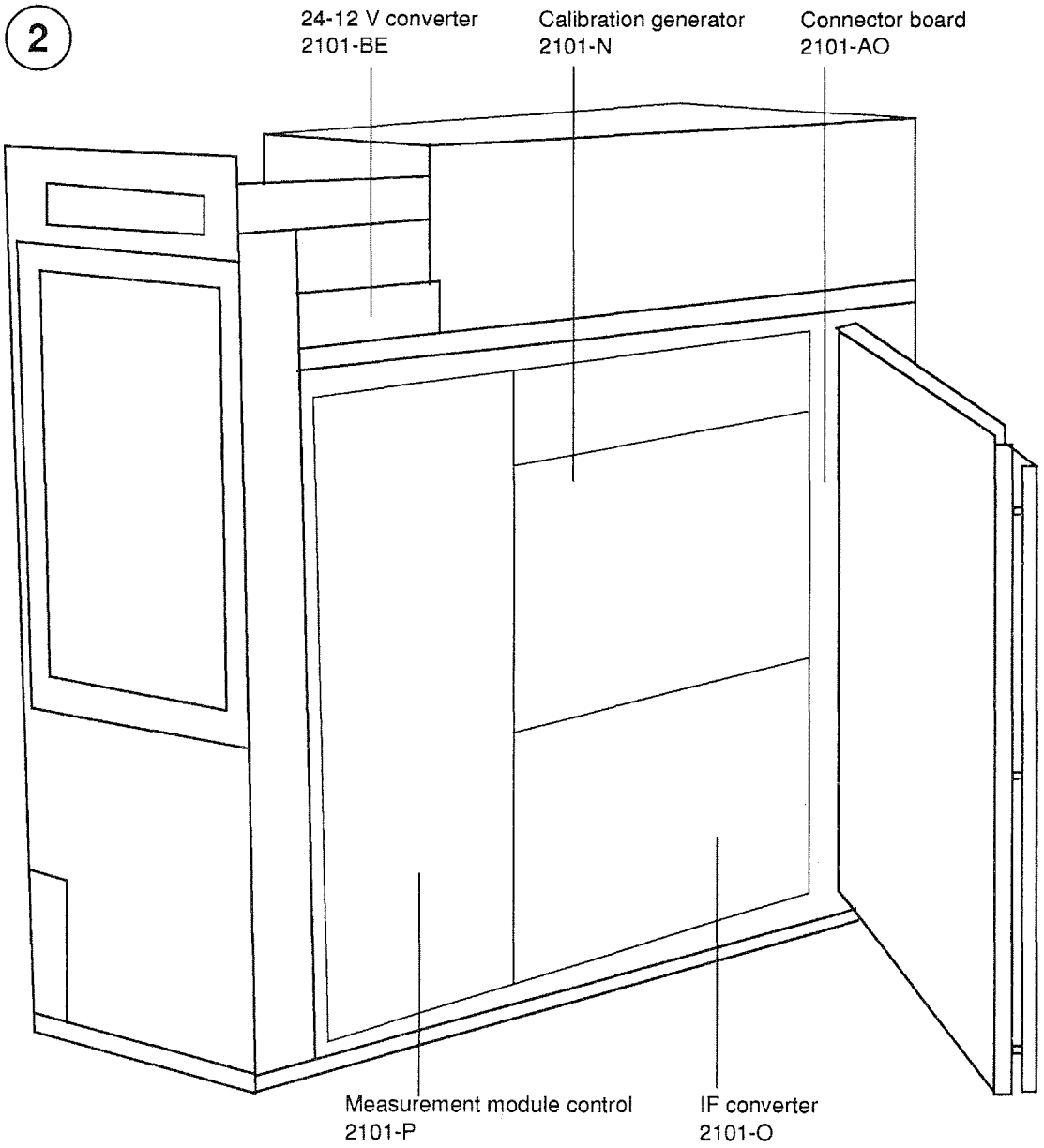


Fig. 3-8 Module positions: Calibration generator, IF converter, Measurement module control and 24-12 V converter

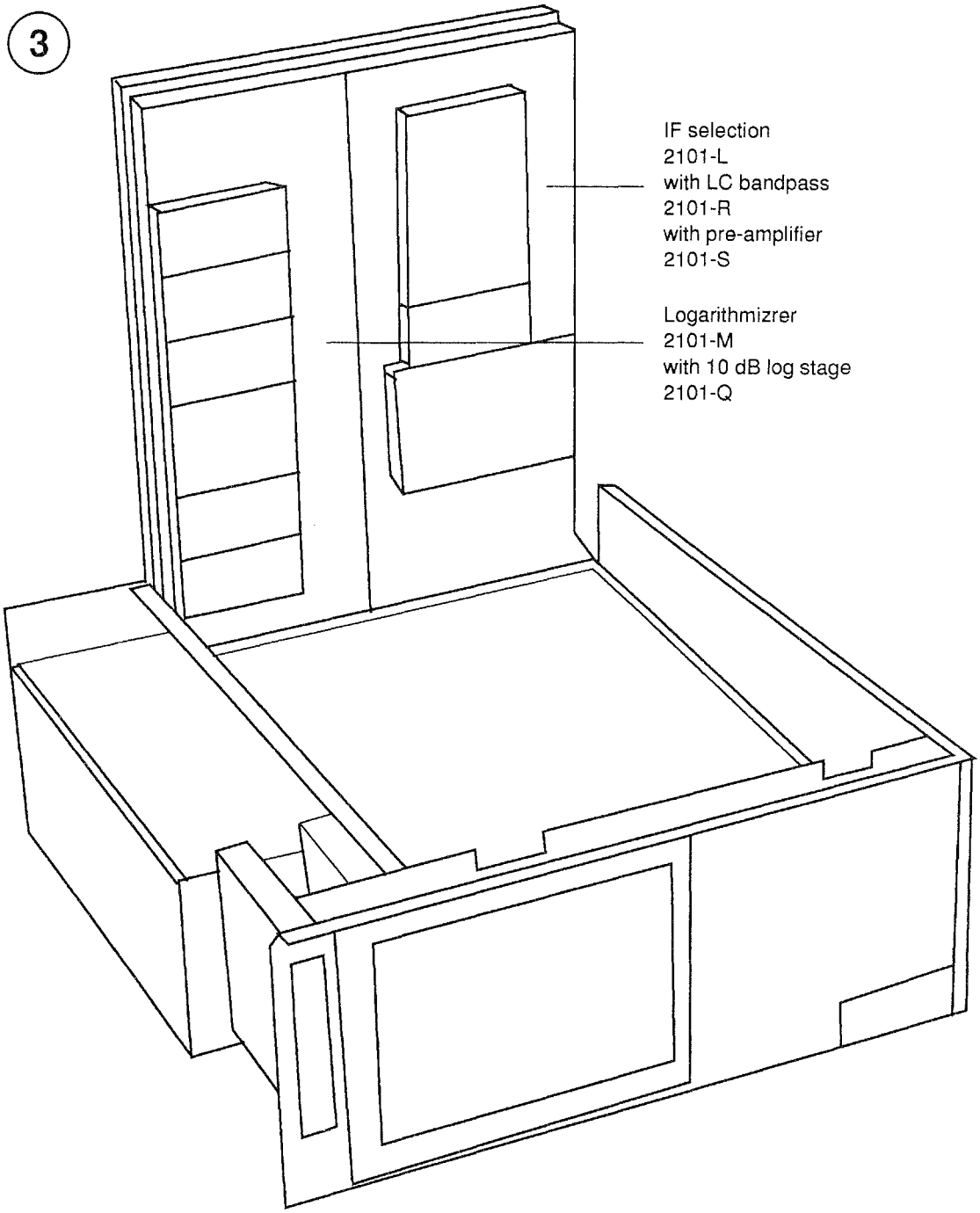


Fig. 3-9 Module positions: Logarithmizer and IF selection

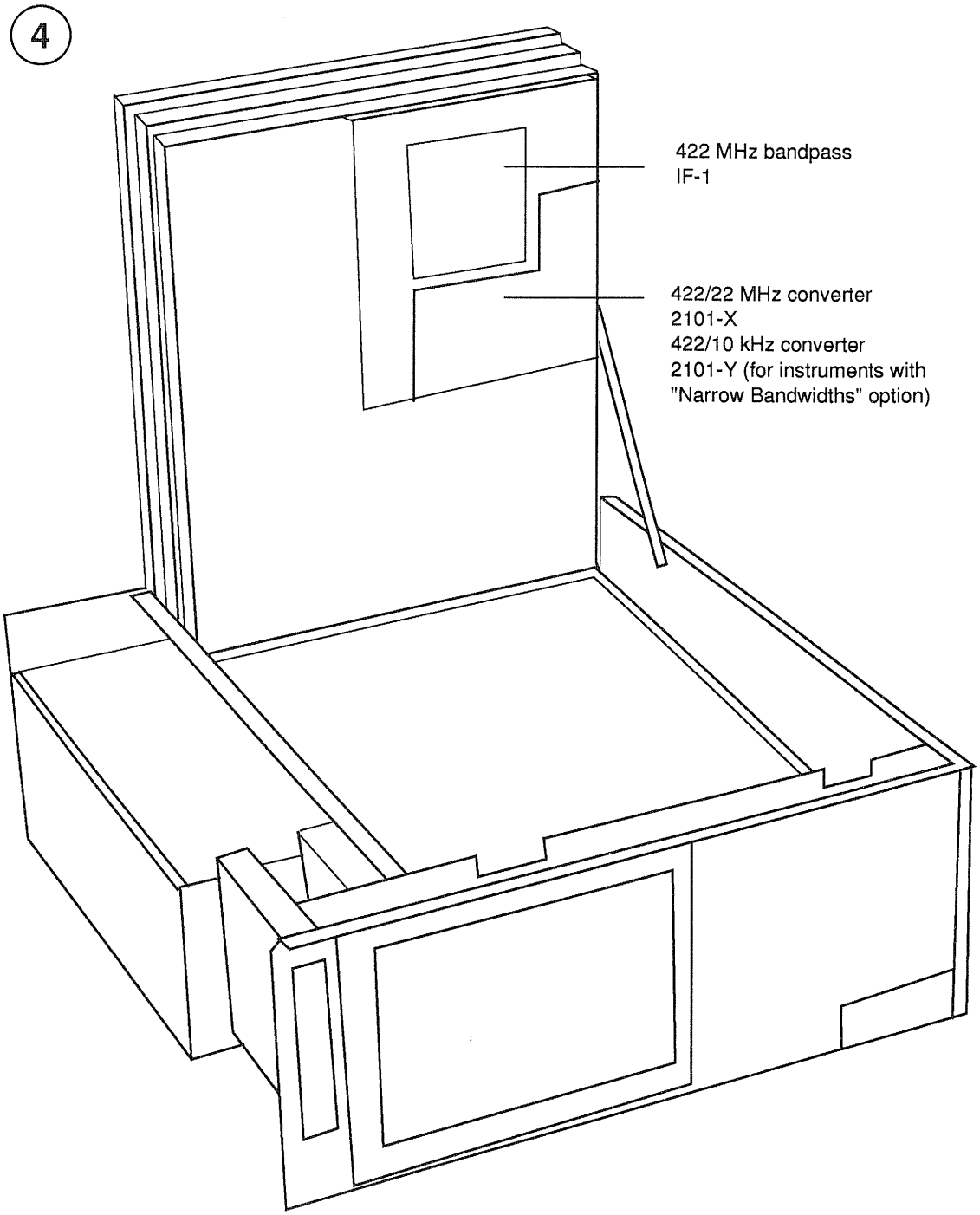


Fig. 3-10 Module positions: 422 MHz bandpass and 422/22 MHz converter

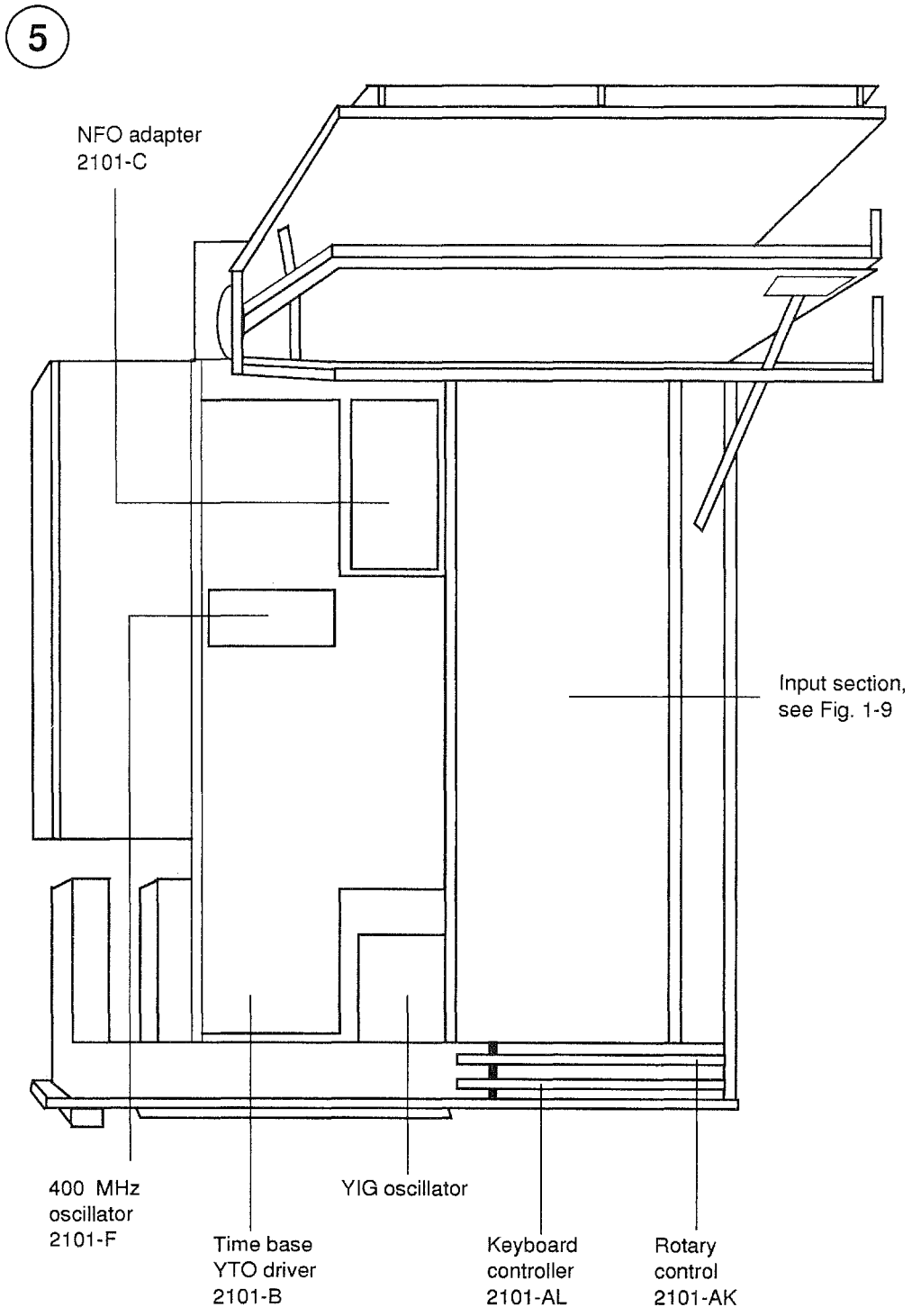


Fig. 3-11 Module positions: OD-11 and input section seen from above

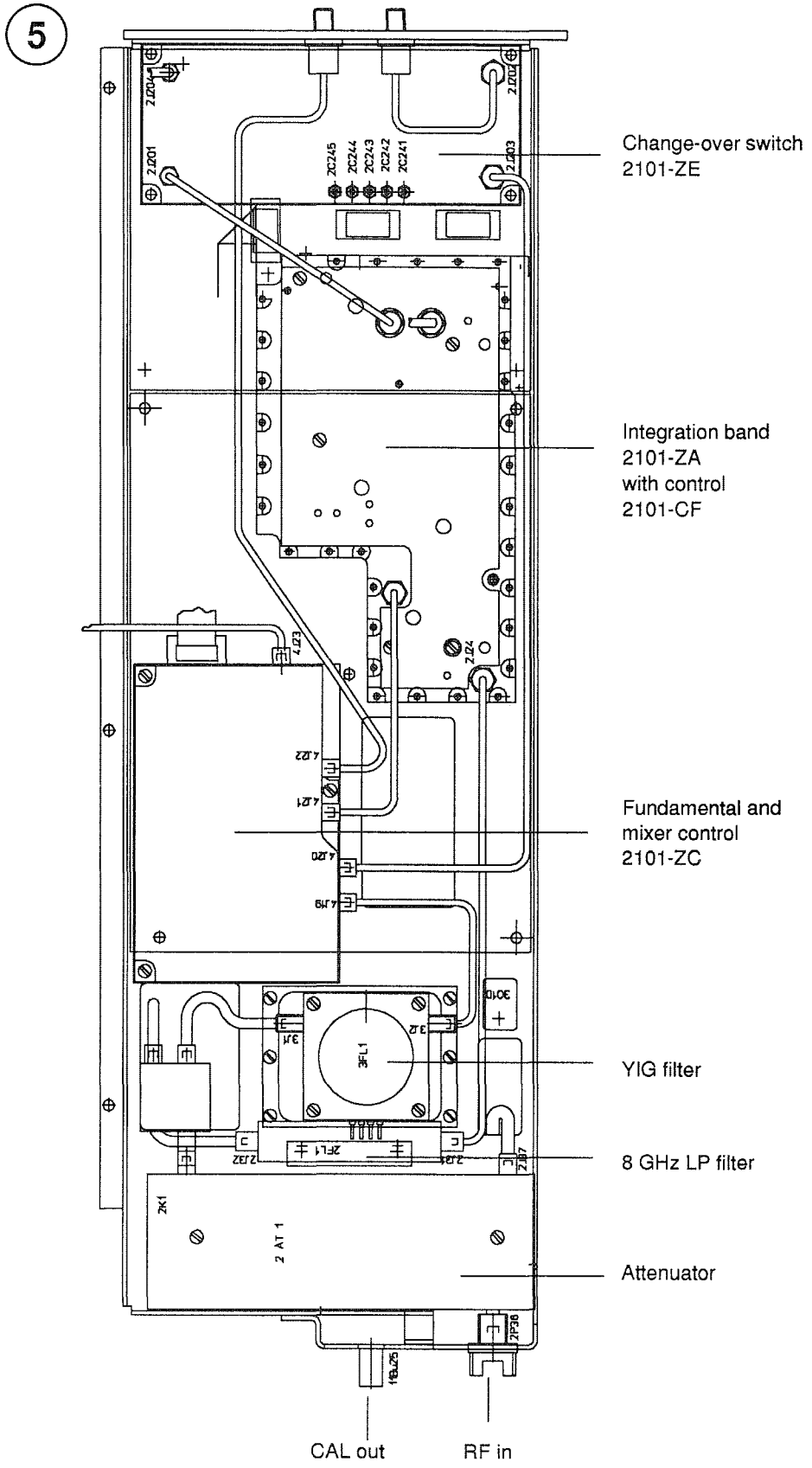


Fig. 3-12 Input section, seen from above

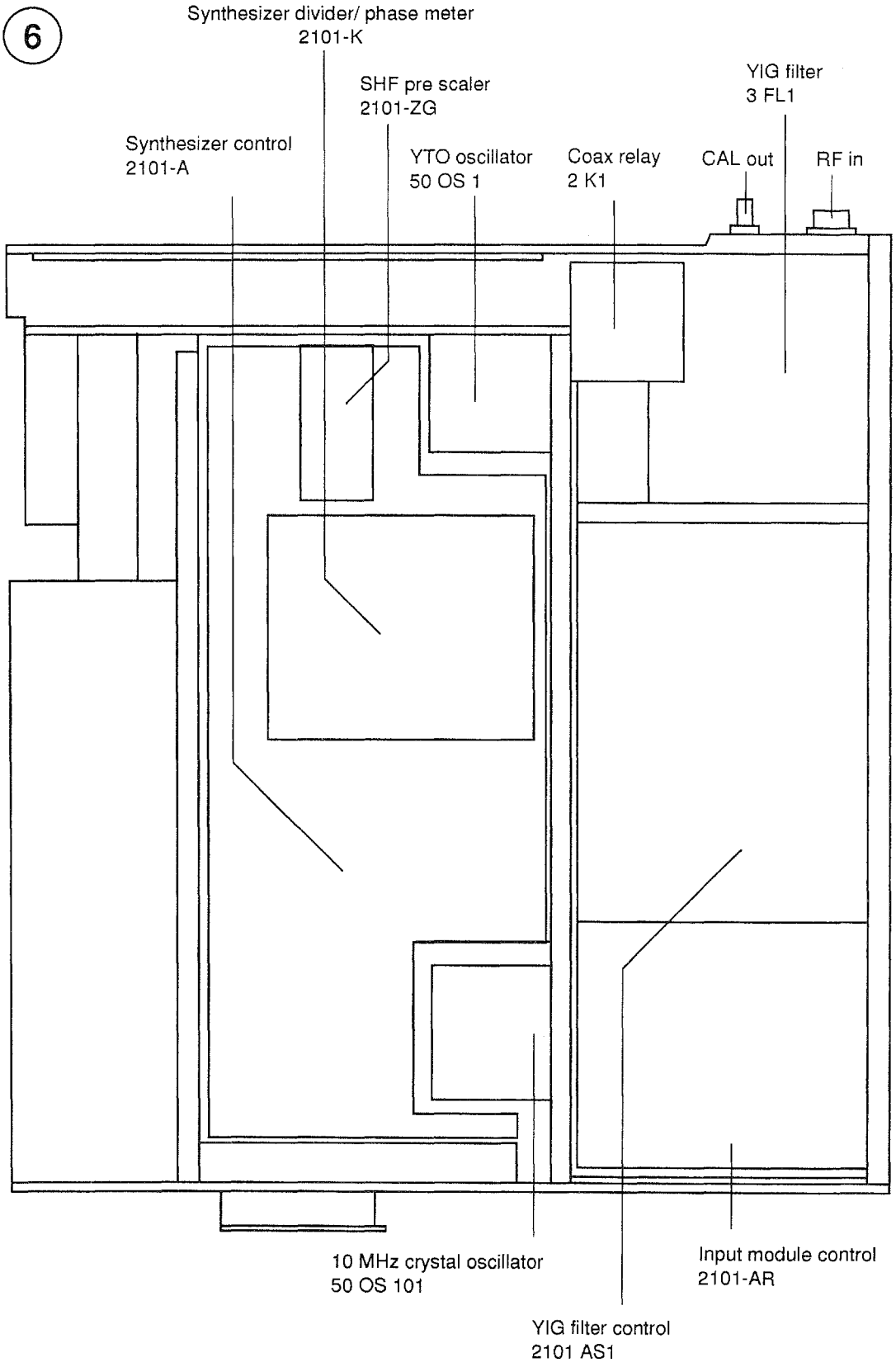


Fig. 3-13 Module positions: OD-11 and input section seen from below

3.2.4 Removing Circuit Boards and Subassemblies

The safety regulations and protective measures described in chapter 2 should be observed when removing circuit boards and subassemblies. In particular, the regulations for "Preventing Electrical Accidents" and the "Anti-static Measures" must be observed.

> ***Caution!***
>
> The memory board contains a battery-buffered RAM in which instrument-specific correction data for the frequency response and logarithmizer are stored along with user setups. A back-up copy of this data must be made before any circuit boards in the region of the memory board are removed, to allow the data to be restored if the RAM power supply is interrupted.

3.2.4.1 Removing Microwave Subassemblies and Modules

When removing microwave subassemblies and modules the following additional measures must be observed:

- "Anti-static Measures" on page 2-3
- "Handling Microwave Subassemblies" on page 2-4
- "Handling the microwave step attenuator line" on page 2-4
- "Handling waveguide lines" on page 2-4

3.2.4.2 Removing the AT-CPU and Memory Boards

Please observe the information in chapter 3.2.4 and chapter 3.2.7.

First remove the aluminium screening cover of the fold-out chassis. To do this, place the chassis in the service position and lock it in position. Then undo a total of 14 cross-head screws. The screen cover can then be lifted off. After this, unplug all the electrical connectors (ribbon cables) connected to the board which is to be removed.
The AT-CPU and Memory boards are connected together electrically only via the two 3-row edge connectors (48-way and 96-way). If one of these boards is to be removed, the screws (spacing bolts) on the other board should also be undone to prevent mechanical stress during the dismantling procedure.
When refitting either of these boards, first mate the dge connectors together carefully and then tighten-up the spacing bolts. This avoids stressing the boards mechanically.

3.2.4.3 Removing the Interface Board and Display Control Board

Please observe the information in chapter 3.2.4 and chapter 3.2.7.

Before either of these boards can be removed, the AT-CPU and Memory boards must be removed (see chapter 3.2.4.2). The interface board and display control board are also linked via two 3-row edge connectors (48-way and 96-way). Use the same procedure for removing these boards as that described in chapter 3.2.4.2.

3.2.4.4 Removing the Power Supply Unit and Voltage Distribution Board

- Remove the instrument chassis from the casing (see chapter 3.2.1)
- Fold out the chassis and lock it in the service position (see chapter 3.2.2)

- Undo the two screws (M4) holding the power supply to the aluminium separator plate (screws C in figure 3-5 on page 3-4)
- Unplug the following connectors from the voltage distribution board:
  ST7, ST8, ST9 St10, BU2, BU3, BU4, BU5, BU6, Bu11 and BU12
- Carefully slide the power supply unit approx. 1 cm towards the front of the instrument, until the steel casing of the power supply is clear of the four tabs on the aluminium separator plate.
- Carefully pull out the power supply unit towards the left-hand side.

To remove the voltage distribution board, first unplug the two connectors ST/BUX1 and ST/BUX2 from the power supply unit and undo the 5 cross-head screws. The circuit board can now be detached from the power supply unit.

3.2.4.5 Removing the Synthesizer

The instrument chassis must first be removed from the casing in order to remove the complete synthesizer or synthesizer subassemblies (see chapter 3.2.1). The subsequent procedures are detailed under the various sub-headings which follow.

Removing the complete synthesizer

To remove the complete synthesizer, including the SHF preattenuator, YTO adapter and NFO adapter, proceed as follows:

- Unscrew and remove the lower part of the printed back panel cover
- Fold out the chassis and lock it in the service position (see chapter 3.2.2 on page 3-3)
- Remove the two cross-head screws on the aluminium separator plate between the Display/Keyboard and Fold-out chassis/Synthesizer (screws D in figure 3-5 on page 3-4)
- Place the instrument on its left-hand side (power supply side)
- Unscrew the waveguide cable between the SHF pre-attenuator (J2) and the fundamental mixer and remove it carefully without bending it.
- Remove the three countersunk screws holding the aluminium fixing brackets between the back panel and the synthesizer (screws located under the previously removed panel cover, screws E in figure 3-5 on page 3-4)
- Unplug the following connectors on the synthesizer control board (51) [2101-A]:
  ST1, ST2, ST3 and ST7
- Unplug ST13 (50ST13) from the time base /YTO driver board [2101-B] (see figure 3-14)
- Unplug the MCX plugs from the following sockets on the time base/YTO driver board [2101-B] :
  BU1, BU3, BU4, BU5, BU7, BU8, BU11 and BU12

The complete synthesizer can now be removed carefully in the direction of the instrument base (first press the synthesizer on the instrument back panel down towards the instrument base).

> ***Important:*** The waveguide between the SHF pre-attenuator (J2) and the fundamental mixer must be unscrewed or reconnected using a torque wrench (e.g. Suhner wrench, order no. 0000-7689.262).

Removing the NFO adapter board [2101-C]

The 10 MHz standard frequency oscillator is mounted (soldered) on the NFO adapter board. The NFO adapter is mounted on the board [2101-B] with three cross-head screws and spacer bolts. Undo the screws (B in figure 3-14) and pull the NFO adapter up to disconnect ST/BU 101.

Removing the time base/YTO driver board [2101-B]

The time base/YTO driver board [2101-B] is mechanically linked to the control board [2101-A]. All of the screws and electrical connectors which must be undone in order to remove the board are shown in figure 3-14 on page 3-17.

- Fold out the chassis and lock it in the service position (see chapter 3.2.2 on page 3-3)
- Remove the NFO adapter.
- Unscrew the three spacing bolts to which the NFO adapter was fitted
- Unplug the connector to the YTO oscillator (ST17)
- Remove the eight cross-head screws (M3, screws A in figure 3-14)
- Unplug ST13 and ST9 from [2101-B]
- Unplug the MCX plugs from the sockets on the time base/YTO driver board [2101-B] (see figure 3-14):
  BU1, BU3, BU4, BU5, BU7, BU8, BU11 and BU12

The circuit board can now be pulled upwards carefully to remove it.

> ***Caution!***
>
> The time base/YTO driver board [2101-B] is stuck to the control board [2101-A] with a strip of conducting aluminium adhesive tape (attached to the screening covers). Lift the tape off carefully on one side when dismantling the assembly. When reassembling [2101-B], make sure that the adhesive tape is stuck back on to the screening covers again.

Removing the synthesizer divider/phase meter board [2101-K]

The synthesizer divider/phase meter board [2101-K] is attached to the control board [2101-K] by eight cross-head screws M3. The electrical connections can only be disconnected when the time base/YTO driver board [2101-B] has first been removed. To remove board [2101-K] proceed as follows:

- Remove the time base/YTO driver board [2101-B].
- Remove the eight cross-head screws on board [2101-K]
- Disconnect the electrical connections to board [2101-K] (MCX plug, ribbon cable and five soldered connections)

Removing the YIG oscillator (YTO)

The oscillator is contained in an aluminium casing for screening purposes. To remove the YTO, this casing must first be removed. To do this, first remove the complete synthesizer, after which the screen and the YTO can be removed.

Removing the 400 MHz oscillator board [2101-F]

The 400 MHz oscillator board [2101-F] is mechanically linked to the time base/YTO driver board [2101-B] by four cross-head screws. The position of the board is shown in figure 3-14 on page 3-17. To remove the board, first remove the screening cover from the frame and undo the four cross-head screws on board [2101-F]. The electrical connection to [2101-B] is by means of 5 solder pins (MT61 through MT65 in figure 3-14). Carefully unsolder these pins before removing board [2101-F].

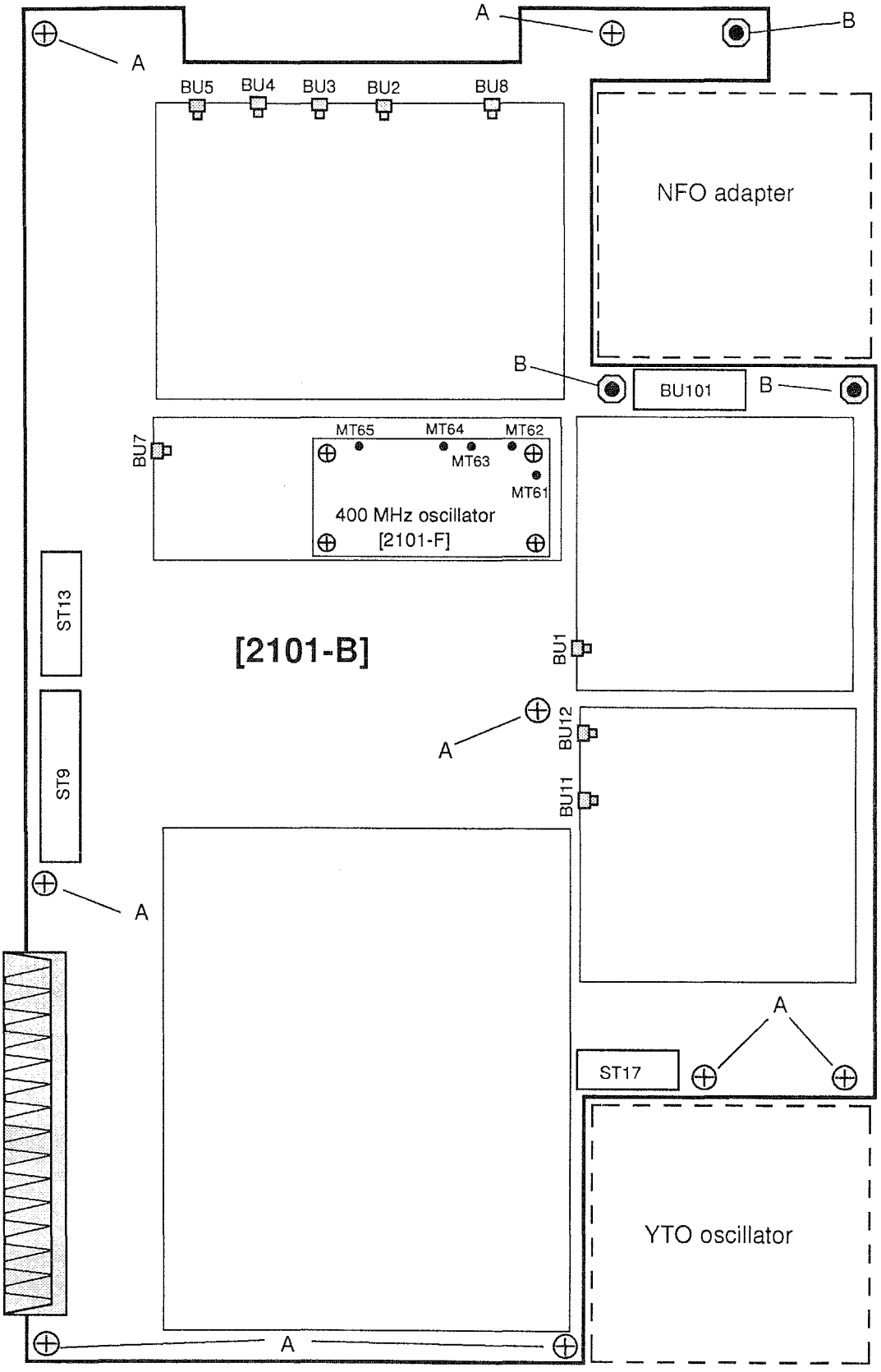


Fig. 3-14 Positions of fixing screws, plugs and sockets on circuit board [2101-B]

3.2.5 Fitting/Removing the Screening Can Covers and Hoods

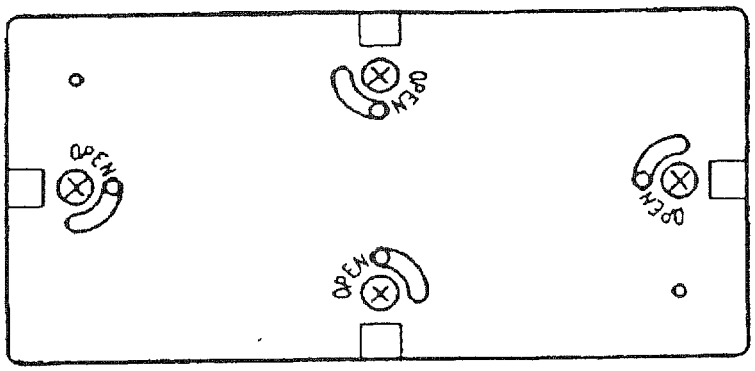


Fig. 3-15 Screening can cover

Opening the cover of the modular screening can

The screening cans are opened with a cross-head screwdriver. The latches are opened by giving the screw about a half turn (pin in the OPEN position).

> ***Caution!***
> If you turn the screw too far, the locking disks may fall off and cause a short circuit.

Closing the covers of modular screening cans

Before replacing the cover on the can, set all latches to OPEN (pin). This ensures that the cover fits tightly on the can giving effective screening. Then close all latches and screw down with a torque of 100 Ncm ± 5 Ncm (torque screwdriver).

Removing the hoods of the modular screening system

The screws in the hoods are removed with a cross-head screwdriver.

Fitting the hoods of the modular screening system

The screws in the hoods are tightened using a torque of 70 Ncm ± 5 Ncm (torque screwdriver).

> ***Important:*** If covers and hoods are not fitted correctly, the instrument may malfunction severely.

3.2.6 Replacing the A.C. Line Fuse

Refer to section 8 of the operating manual under the heading "Changing the fuse".

3.2.7 Replacing the Memory Buffer Battery

A lithium battery is plugged on to the memory board (17). This battery provides power for buffering the RAM when the instrument is switched off. The RAM contains the instrument-specific correction data and the user setups, among other things. If the lithium battery is removed when the instrument is switched off, this data will be lost within a few seconds.
If the battery is to be replaced as a precaution during repairs (average battery life is about 5 years) the user setups should first be saved on a floppy disk (see chapter 4.8) .

> ***Caution!***
>
> Before replacing the battery, make sure that the "Compensation Data Disk" belonging to the instrument is available and free of errors, so that the correction data tables can be re-loaded into the RAM after the battery has been replaced (see chapter 4.7). If the "Compensation Data Disk" is not available, a back-up copy of the RAM disk (battery-buffered RAM) must be made so that this can be copied back into the RAM disk after replacing the battery (see chapter 4.9).

4 Power-On Test, Error Messages, Software Configuration

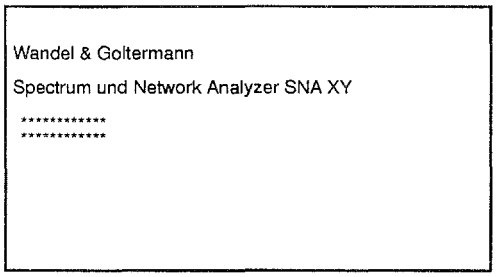
4.1 Normal SNA Boot-Up Behavior (Series A to E)

The power-on (boot-up) behavior of the SNA-20/-23 is described below. The following conditions must be fulfilled for the instrument to behave as described:

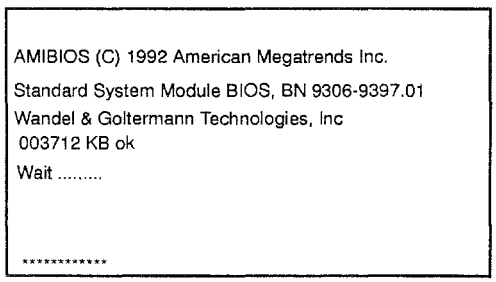
- Instrument must be from series A through E (fitted with CPU "STANDARD SYSTEM MODULE 386_WGR" (3011.9305.006)).
- Instrument is OK (no faults detected during switch-on (BIOS) test).
- There is no (bootable) disk in the SNA-20/-23 floppy drive.
- No key is pressed on the built-in or external keyboard during the boot-up procedure.

The following messages are displayed on the screen after switching on if these conditions are met. Short descriptions of the actions currently being performed by the SNA are shown to the right of the screen messages.

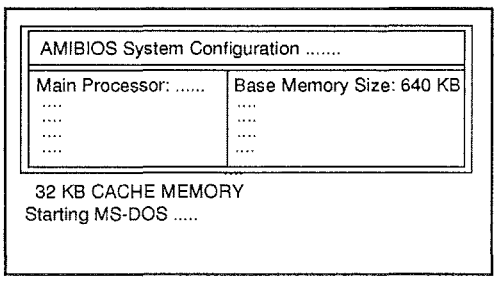
Note: The messages displayed may differ slightly from those depicted here, as they depend on the display board and AT-CPU BIOS versions used.



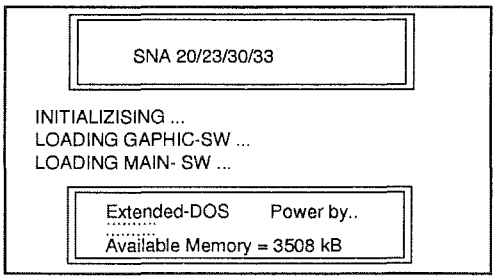
After power-on, the AT-CPU loads the VGA BIOS (BSK-3) and the extended BIOS for the memory board (17). If the memory board extended BIOS loads successfully, the AT-CPU can access drives C: (Flash ROM disk) and B: (battery-buffered SRAM segment on the memory board). This automatically starts the BIOS test (POWER-ON TEST).
The crossover switch on the display control board (BSK-3) is set to VGA ---> EL. This means that all output to the built-in EL display is generated by the VGA module on the display control board (BSK-3). Output to any externally connected monitor is via the graphics processor (TI processor) of the BSK-3.



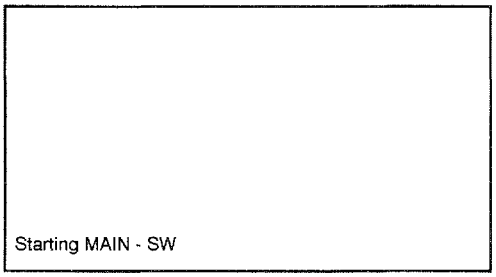
The BIOS test takes about 10 s to complete. If no faults are detected, a single long beep is output. If errors have been detected, appropriate error messages are displayed if this is possible. Otherwise, audible warning is given (see chapter 4.2).



The AT-CPU configuration detected during the BIOS tests and as set in the CMOS setup is displayed. The operating system (DOS) is then loaded from the memory board (flash ROM).



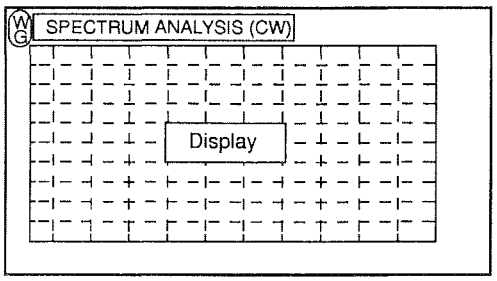
The AUTOEXEC.BAT file on drive C: is processed. The graphics software and instrument software are then loaded from the memory board (flash ROM). A memory manager (extended DOS) is loaded to allow the the operating system and instrument software to use the memory area above 640 kB.



The instrument (measurement) software is started.

If the instrument software starts correctly, a beep is output.

After starting the "main" software, the crossover switch on the display control board (BSK-3) is switched to the VGA ---> CRT setting. This means that the subsequent output to the EL display is generated by the graphics processor (TI processor of the BSK-3). The output to any externally connected monitor is via the VGA module of the BSK-3 from now on.



The measurement display is shown. The instrument is ready for use.

Fig. 4-1 Screen displays during normal boot-up (power-on) of the instrument

4.2 BIOS-Test (Power-On Test) Error Messages [Series A to E]

A power-on test (AT-CPU BIOS test) is performed when the instrument is switched on (compare chapter 4.1, "Normal SNA Boot-Up Behavior (Series A to E)"). The tests performed and the error messages which may be displayed depend on the AT-CPU (BIOS version and manufacturer) used in the SNA. The following refers to the AT-CPU "STANDARD SYSTEM MODULE 386_WGR" (3011.9305.006) used in instruments from series A through E .

The BIOS test checks practically all of the functions of the AT-CPU. The basic functions of the following modules are also tested:

- Display control board
- Keyboard controller
- Floppy disk drive

The value of the BIOS TEST is somewhat limited due to the bus system used (CONTROL BUS). In addition to the above-mentioned boards, the memory and interface boards are also connected to this bus. If one of the boards causes a bus conflict, the result of the BIOS test does not allow identification of a defective module.

If an error occurs during these tests, audible and visual warnings are output. These are useful for tracing faults in the control unit. Attention should be paid to the audible warnings (duration and sequence of beeps) which may occur during the boot-up procedure (immediately after switching on).

The self test (BIOS TEST) has been completed successfully when a long BEEP is heard (see "Normal SNA Boot-Up Behavior (Series A to E)" on page 4-1)

After this, the instrument software is loaded automatically.

The following indicates how faults in the control unit can be traced; examples of possible error conditions and their causes are used for this.

Note: It is assumed that the supply voltages for the instrument are correct for the following troubleshooting procedure. It is therefore a good idea to check the supply voltages to the control unit circuit boards first (see block diagram in Service Manual Annex).

Electroluminescent display remains blank after switch-on - audible warnings

Beep sequence: 1 x long beep approx. 10 seconds after switching on

The beep indicates that the BIOS has been completed successfully. The fault is therefore either in the display control board (BSK-3) or in the EL display. The function of the display control board can be checked by connecting an external monitor. If the monitor screen also remains blank, the display control board is faulty. Otherwise, the EL display DS1 must be checked for faults or the complete unit (16) exchanged.

Important: The external monitor only shows a display if the crossover switch on the display control board (BSK-3) switches from the VGA module to the TI graphics processor (GSP) for the EL display. This occurs when the measurement display is or would normally be shown on the built-in EL display (see "Normal SNA Boot-Up Behavior (Series A to E)" on page 4-1).

Beep sequence: 1 x long and 3 x short; 1 x long and 8 x short

A fault was detected on the display control board during the test (e.g. the VGA BIOS for the BSK-3 could not be loaded). Clear the fault by replacing the display control board (BSK-3).

Beep sequence: 3 x long

A fault occurred during the test of the first 64 kB of the RAM on the AT CPU. Clear the fault by replacing the AT CPU.

Electroluminescent display lights up (normal boot-up) - audible warnings

Beep sequence: continuous sequence of short beeps

The instrument boots-up normally until the message "Starting MS-DOS" appears. The long beep (indicating a successful BIOS test) is **not** output and the instrument software is **not** loaded.

This fault condition indicates an error during the keyboard test. Possible causes are a stuck key or a fault in the keyboard controller.

Other possible fault conditions

The BIOS test displays an error message on the EL display. Most of the tests apply to the AT CPU itself. The remaining tests apply to the display control board, the keyboard controller and the floppy disk drive. The error messages indicate which of these modules is the likely source of the fault.

4.3 Error Messages / Faulty Behavior After Successful BIOS Test (Series A to E)

Introduction

After the BIOS test, first the operating system (DOS) and then the instrument software will be loaded and started. The operating system and the instrument software are both stored on drive C:, which is the memory board (FLASH ROM DISK). The SNA's AT-CPU configuration has this drive (C:) set as the BOOT drive (set in the extended BIOS which is also loaded from the memory board FLASH ROM DISK). If the AT CPU cannot "find" the extended BIOS, e.g. due to a defect on the memory board, the operating system can be loaded from a bootable floppy disk.

If the AT CPU loads the extended BIOS, the operating system can only be loaded from a floppy disk if this is labelled "WAGO_BOOT". The service disk can be used in such cases.

Note: If errors occur during loading of the instrument software or during measurements, first check the settings in the CMOS setups for the AT CPU (see chapter 4.5 on page 4-9).

Operating system/instrument software does not load

Operating system does not load

If the memory board (17) is not detected during the BIOS test (extended BIOS is not loaded), drive C: does not exist for the SNA. The instrument behaves like a normal PC and attempts to load the operating system from the floppy drive (drive A:).

Error message:	**DRIVE NOT READY ERROR** insert BOOT diskette in A: Press any key when ready
Possible causes:	Memory board (17) defective, FLASH EPROMS U400, U401 on memory board (17) completely or partially erased or defective. Error in control unit (e.g. CONTROL BUS conflict)
Remedy:	To locate the error, first boot the SNA from a floppy disk (e.g. service disk). If the operating system loads from the disk, the prompt A:\ is displayed. Next, try to re-install the instrument software from the floppy disks. If this is not possible, the memory board (17) should be repaired or replaced and the software re-installed. If the SNA will not boot from the floppy disk, the fault is in the control unit.
Error message:	**General failure reading drive B** Abort, Retry, Fail?
Note:	This error message indicates that the data and compensation tables stored on drive B: are faulty or have been erased (see chapter 4.7 on page 4-15).
Possible causes:	SRAM (drive B:) on the memory board (17) defective, lithium battery on the memory board (17) defective.
Remedy:	To locate the fault, first check the lithium battery on the memory board. Then place the "Compensation Data" disk in drive A: and switch on the SNA. The operating system is loaded from the disk and the compensation data are copied into the RAM disk (drive B:). If this is not possible, the memory board should be replaced or repaired, after which the compensation data and the instrument software should be reinstalled (see chapter 4.6 on page 4-14). If the SNA will not boot from the disk either, the fault is located in the control unit.

Operating system/instrument software does not load

If the memory board (17) is detected during the boot-up procedure (extended BIOS is loaded), the SNA attempts to load the operating system and then the instrument software from drive C:. If errors occur, various error messages may be output or the SNA may lock up completely. As a check that the extended BIOS has loaded, attempt to access drives C: and B: from the DOS prompt by entering the DOS commands <C:> or <B:> followed by <dir>. If the drive directory is displayed, the extended BIOS has been loaded from the memory board.

Possible causes:	Memory board defective, FLASH EPROMS on memory board (17) partly or completely erased or defective.
Remedy:	To locate the fault, first boot the SNA from a disk (e.g. service disk). If the operating system loads from the disk, the prompt A:\ is displayed. Now try to reinstall the instrument software from disk (see chapter 4.6 on page 4-14). If this is not possible, repair or replace the memory board and then reinstall the instrument software. If the SNA will not boot from the disk either, the fault is located in the control unit.
Note:	The above error scenario indicates that at least part of the memory board is working correctly as the extended BIOS could be loaded from U400 and U401 on the memory board. If this were not the case, the error message DRIVE NOT READY ERROR would appear.

4.4 Error messages during measurements

If a major hardware fault occurs after the instrument software has been loaded or during measurements, the measurement program is aborted and appropriate error messages are displayed on the screen ("2101 Debug Output" is displayed). The error messages allow localization of the fault in a limited sense.

4.4.1 2101 Debug Output

If a so-called Fatal Error occurs during operation of the SNA, the instrument software aborts and the message "2101 Debug Output" is displayed. Figure 4-2 shows an example of the 2101 Debug Output message. The error messages are shown in boldface type. The SNA is in DOS mode after exiting from the operating software.

```
                    BN2101 debug output
selector of main() = 0x017F                                    14:34:31
2194316 Bytes of memory available
main: starting
1663956 Bytes of memory available

INTERNAL ERROR <0>: Download error ZF-DSP 0x3000
CommunicationError from ZF-DSP in ZF_Get_PegKorrLoc. ErrorCode = 3005
Error 3005: ZF_Get_PegKorrLoc
Error 3005: WriteRam from daten_tablog not ok!
Error 3005: WriteRam from daten_tablin not ok!
INTERNAL ERROR <0>: Download error Synthe 0x3000
CommunicationError from ZF-DSP in ZF_Set_Vbw. ErrorCode = 3005
FATAL ERROR <3005>: ZF_DSP_Error in ZF_Handler
program terminated at                                          14:34:42
C:\
```

Fig. 4-2 Example "2101 Debug Output" display

A large number of Internal Errors may occur and be displayed before the instrument software is terminated by a "Fatal Error". These Internal Errors are useful in tracing the cause of a fault as they can indicate the cause of the subsequent Fatal Error and hence the cause of program termination. The events leading up to a Fatal Error are therefore of interest in troubleshooting. Evaluation of the 2101 Debug Output message must always begin with the first error message displayed.

Note: The display of the SNA cannot be scrolled in this mode. If a large number of errors have occurred, it is possible that the screen will only display the last error messages before the fatal error. The header line of the 2101 Debug Output page indicates whether some messages have been overwritten or not. If the header "2101 Debug Output" is still visible at the top of the display, this means that all of the error messages are displayed. If this header is no longer displayed, some of the messages have been overwritten and cannot be displayed.

The entire contents of the 2101 Debug Output message are also stored in the file B:\SNA.ERR so that all of the error messages can be read even if they do not fit onto a single display page.

Displaying the contents of the file B:\SNA.ERR

The instrument is in DOS mode when the instrument software is aborted by an error. The "2101 Debug Output" message is displayed, followed by the DOS prompt C:.

Important: Connect an external keyboard for making the following entries.

Now make the following entries in the order given, confirming each entry by pressing Return:

– B:	Switch to drive B (RAM disk, battery buffered RAM on the memory board).
– TYPE SNA.ERR|More	This displays the complete contents of the file SNA.ERR page by page on the display. The character | is obtained by simultaneously pressing [Alt Gr] + [<,>] on the external keyboard.

> ***Caution!***
>
> The contents of SNA.ERR will be overwritten by the error messages occurring during the new boot-up if the SNA is switched off and then on again. The original error messages will be lost if different errors occur during the new boot-up procedure.

The contents of SNA.ERR can be displayed more conveniently by using the DOS editor. Enter EDIT to load the editor. Open the file B:\SNA.ERR to display it. The file can be printed out from the editor.
You can also save the file B:\SNA.ERR to a disk in drive A: by using the "SAVE AS" command in the "FILE" menu of the DOS editor.
This file can then be read and printed out using any PC with a word processor program.

Important: See the DOS manual for details of how to use the editor function.

4.5 AT CPU CMOS Setup (Series A to E)

4.5.1 Introduction

The correct CMOS setup is necessary for the SNAs processor (AT CPU) to operate correctly. The settings are stored in a battery-buffered RAM module in the AT CPU (the RAM module and battery are part of the AT-CPU clock module) . The setup program uses menus (in English) The following settings are possible (required) for the STANDARD CMOS SETUP for the CPU used in the SNA:

- Date: mn (month)
  date
  year
  (the day of the week is entered automatically from the date)
- Time: hour
  min
  sec
- Hard Disk C: Type: } Number from a table predefining the hard disk parameters.
  Hard Disk D: Type: } Enter no. 47 to select a user-defined hard disk.
  If this is done, all disk parameters (Cyln, Head, WPcom etc.) must be entered manually.
- Floppy Drive A: } Type (capacity) dof the floppy drive installed
  Floppy Drive B: }
- Primary Display: Type of graphics board installed.
- Keyboard: Selects whether keyboard test is performed during boot-up or not.

The size of the DRAM on the CPU (BASE MEMORY, Ext. Memory) is determined during booting of the CPU and is entered in the appropriate menu fields. These values cannot be altered.

Settings affecting the hardware for the AT-CPU must be made using the ADVANCED CMOS SETUP program. The SNA only allows setting of the "Shadow RAM Option".

4.5.2 Invoking the CMOS Setup Program

The AT CPU CMOS setup program can be started in various ways. Different methods are used to access the CMOS setup menu, depending on whether an external keyboard is connected to the SNA or not.

Invoking the CMOS setup program using an external keyboard

With the SNA switched off, connect an external keyboard to the SNA. Press and hold down the Delete key on the external keyboard, and switch on the SNA. Hold the Delete key down until the setup menu appears (see fig. 4-3).

Invoking the CMOS setup program using the built-in instrument keyboard

Switch on and wait until the message "Wandel & Goltermann, Spectrum and Network Analyzer SNA XY" is displayed. Then press and hold down the the DEL key of the instrument until the setup menu appears (see fig. 4-3).

Note: The message "Hit <DEL> If you want to run SETUP" appears briefly. DEL must be pressed before this message disappears, otherwise the instrument will not branch to the setup program and the instrument software will be loaded (see "Normal SNA Boot-Up Behavior (Series A to E)"). If the instrument software loads, switch off the SNA and try again.

Setup menu display

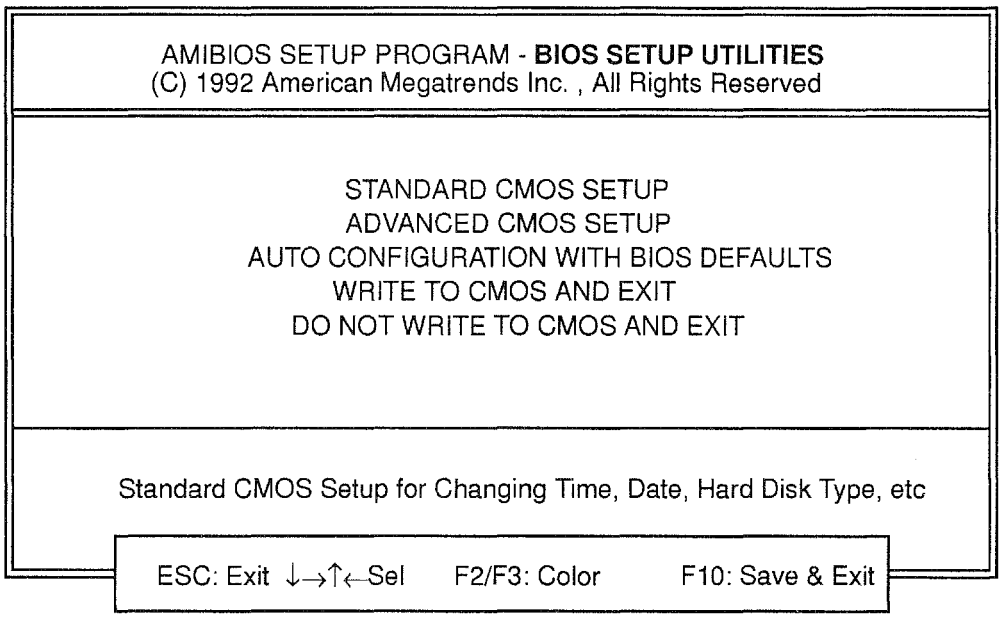


Fig. 4-3 Screen display after invoking the setup program

Figure 4-3 shows the (initial) setup menu. The bottom line of the menu containing the operating hints is not visible on the built-in EL display of the SNA. For this reason, all of the more important setup menu displays are reproduced in the figures which follow.

4.5.3 Using the CMOS Setup Program

Using an external keyboard

See chapter 4.10 for connecting an external keyboard.

If the setup menu is displayed (see fig. 4-3) the cursor keys ↓→↑← can be used to select the various menu items (STANDARD CMOS SETUP, ADVANCED CMOS SETUP etc.) When the RETURN key (↵) is pressed, the program branches to a warning menu which indicates the consequences of making an incorrect entry in the setup. Pressing RETURN (↵) again displays the sub-menu which was selected.

The keys have the following functions when an external keyboard is used to operate the setup program:

Cursor keys ↓ → ↑ ← :	Select menu item / field
PgUp, PgDn:	Change field content / Select option
ESC:	Return to initial menu
Return ↵ :	Invoke / confirm selection made

Using the built-in keyboard

The keys have the following functions when the built-in keyboard is used to operate the setup program:

↓ ↑ :	Select menu item / field
ZOOM ↔ :	Change field content / Select option
ESC:	Return to initial menu
Enter:	Invoke / confirm selection made
SWEEP:	Y (YES)
HOLD:	N (NO)

4.5.4 SNA-20/23 CMOS Setup Settings

STANDARD CMOS SETUP

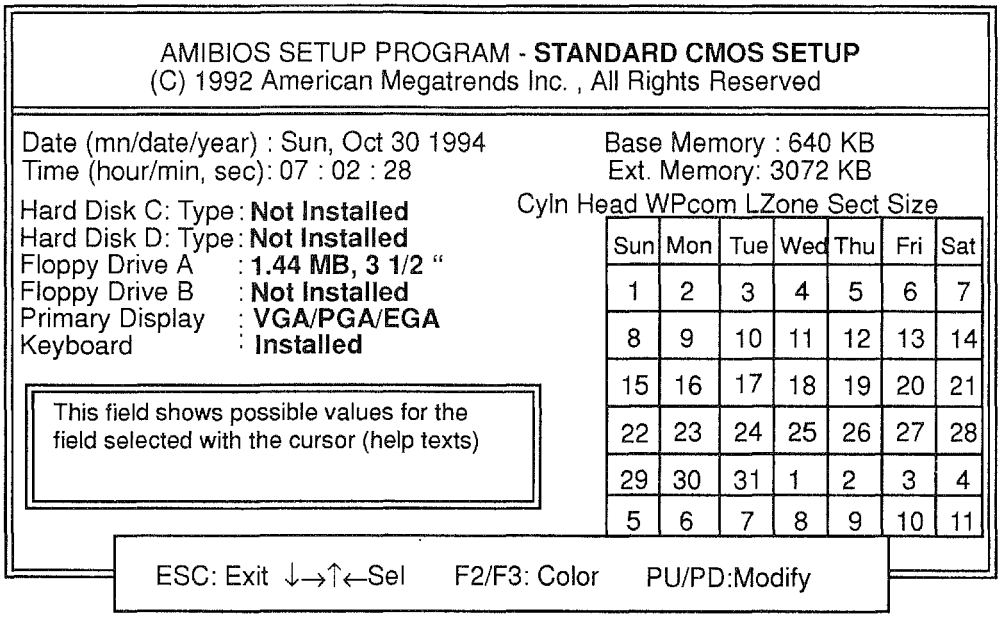


Fig. 4-4 Standard CMOS Setup values and options (Series A to E)

Figure 4-4 shows the STANDARD CMOS SETUP sub-menu. The values entered in the menu (shown in boldface type) are the values prescribed for the SNA and must be set to these values for the SNA to function correctly, with the exception of the date and time values which should be set to the appropriate current date and time.
The help text window shows possible settings, options and explanantions for the field selected by the cursor.

ADVANCED CMOS SETUP

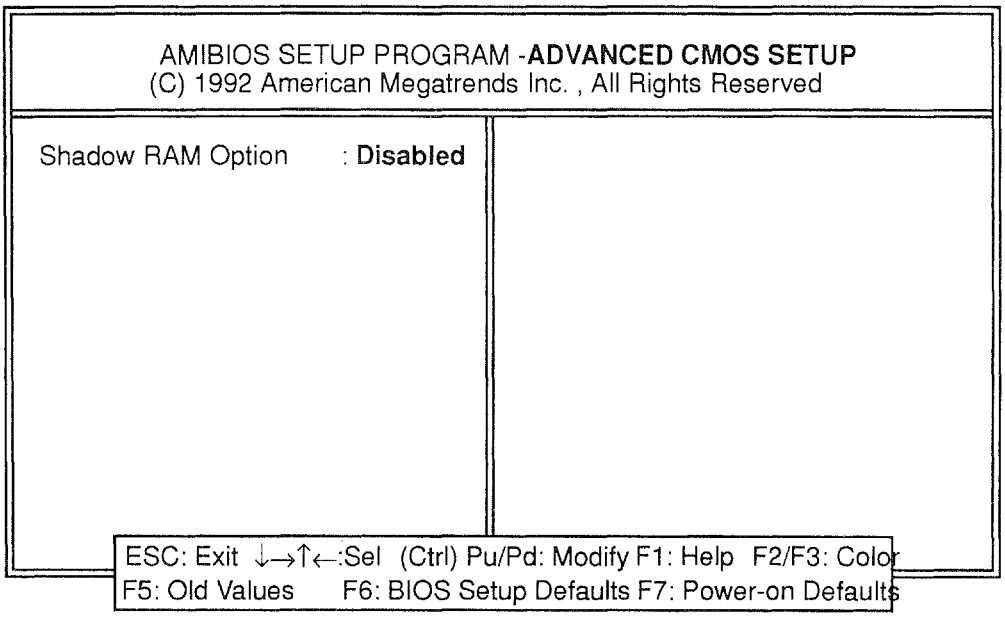


Fig. 4-5 Advanced CMOS Setup values and options (Series A to E)

The SNA ADVANCED CMOS SETUP (see fig. 4-5) only allows setting of the "Shadow RAM Option". The "Disabled" setting must be selected to ensure that the instrument operates correctly.

4.5.5 Ending the Setup Program

Once all the settings are correct, the program can be terminated. If setup settings were changed (corrected), terminate the program using the "**Write to CMOS and Exit**" command.

Exit without saving

If no settings were altered, exit the program using the "DO NOT WRITE TO CMOS AND EXIT" command. Press the ESC key to return to the initial menu and then select this menu item (see below under "Using a country-specific external keyboard").

Exit and save

If settings were altered, you must exit the program using the "WRITE TO CMOS AND EXIT" command to write the changes to the CMOS RAM of the CPU for them to become effective (see below under "Using a country-specific external keyboard").

Using a country-specific external keyboard

When exiting from the setup program, the program requests a N (No) or Y (Yes) response before the program can be ended. The setup program uses the US-standard keyboard driver. If you are using a non-US keyboard, some of the key functions may be different (e.g. on a German keyboard, the positions of the **"Z" and "Y"** keys are reversed). Press the key on your keyboard which corresponds to the "N" or "Y" key on the US keyboard to respond to the exit query. This does not affect the use of the built-in keyboard (see "Using the built-in keyboard" on page 4-11).

Please also refer to chapter 4.10.

4.6 Installing the Instrument Software / Updating Software

The instrument software will need to be installed if the memory board is replaced or repaired. Insert disk no.1 in the floppy drive (A:) of the SNA and switch the instrument on. The software is installed automatically. From time to time during the installation, you will be asked to confirm various messages by pressing a key. The screen also indicates when the next floppy disk is to be inserted (the disk number will be displayed). The instrument software is stored on drive C: (Flash ROM disk).

Use the same procedure for installing software updates.

The compensation data for the instrument (see chapter 4.7) and any user-specific settings or setups are not affected by loading the instrument software, as they are stored on drive B:\ (battery-buffered SRAM on the memory board (17)) of the SNA. If these files are lost or damaged, they must also be reinstalled (see chapter 4.7).

4.7 Installing the Compensation Data

The extreme accuracy of the SNA-20/-23 can only be achieved by calibration of various circuit modules and subassemblies. This compensation data is stored in the form of tables in the instrument and is used to correct measurements during operation of the SNA. A floppy disk containing a backup copy of the the compensation data specific to the instrument is included with each SNA.
The following compensation data is determined and stored for each individual SNA:

- Frequency response correction, Band 0 File: SNA\DATA\ fckor_b0.tab
- Frequency response correction, Band 1 File: SNA\DATA\ fckor_b1.tab (SNA-23)
- Frequency response correction, Band 2 File: SNA\DATA\ fckor_b2.tab (SNA-23)
- Frequency response correction, Band 3 File: SNA\DATA\ fckor_b3.tab (SNA-23)

- Logarithmizer correction, linear File: SNA\DATA\ pkor_lin.tab
- Logarithmizer correction, logarithmic File: SNA\DATA\ pkor_log.tab

Instruments with memory board (17) [Series A to E]

The specific compensation data are stored on RAM disk (battery buffered SRAM on the memory board (17)). The RAM disk is drive B:\. The compensation data will need to be reinstalled if this board is repaired or replaced, or if the Lithium battery on the board fails. Insert the "Compensation Data" disk in floppy drive A:\ of the SNA and switch on the instrument. The installation of the files is then automatic. During installation, a message appears to indicate that all user-specific settings have been lost. Once you confirm this message by pressing any key, drive B:\ is formatted and the required data are copied from drive A:. Once this has been completed, remove the floppy disk from drive A: and press any key to reboot the SNA automatically.

> ***Caution!***
> Loading the compensation data deletes all user setups. If such information is stored in the instrument, make a back-up copy of it before installing the compensation data (see chapter 4.8 on page 4-15).

4.8 Saving User Setups on Floppy Disk

Before making repairs to the instrument, user-specific intrument settings (setups) should be backed up to floppy disk. This is particularly important if the memory board (17) is to be repaired or replaced or if the Lithium battery on this board is replaced.
Insert a formatted disk in drive A:\ of the SNA. In the MODE/DOS UTILITIES menu, press the BACKUP RAM SETUPS TO FLOPPY softkey to save the user setups to the floppy disk.

Once repairs have been completed, the setups can be restored to the RAM from the same menu. Switch on the instrument and insert the floppy disk containing the saved setups into drive A:\. Press the RESTORE RAM SETUPS FROM FLOPPY to read the setups from the disk and write them back to the battery-buffered RAM in the SNA.

4.9 Making a Back-Up Copy of RAM Disk B:\

(Applies only to instruments fitted with memory board (17) [Series A to E])

If the "Compensation Data Disk" is not available, a back-up copy of the complete contents of RAM disk (B:) can be made on a floppy disk. Data can then be restored from this disk e.g. when the battery is replaced. To make the back-up copy, do the following:

- Connect an external keyboard to the SNA
- Switch on and wait until the measurement display appears on the SNA screen
- Press <ALT>+ <F10> simultaneously to switch back to DOS mode. Press <RETURN> to display the DOS prompt C:\>.
- Insert an empty, formatted disk in drive A: of the SNA
- Use the external keyboard to enter the DOS command XCOPY B:*.* A:\ /e and then press RETURN. The entire contents of drive B: including all subdirectories will be copied to the disk in drive A:.

This disk now contains all compensation data and the user setups contained in drive B:. This procedure should be followed whenever data might be lost during repair of the instrument and the "Compensation Data Disk" for the particular instrument is not available. This is particularly the case if the battery is to be replaced during repairs or if repairs are made to the AT CPU, display control board, interface board or memory board.

Retrieving the back-up to the RAM disk (B:)

- Insert the service disk in drive A:\ and switch on the SNA (the instrument boots from the disk and the DOS prompt A:\> is displayed).
- Enter the following from the external keyboard: FORM_B. Then press RETURN.
  The message

  Escape with "ENTRY OFF" (Press ENTRY OFF on the built-in keyboard
  Continue with any key to stop the procedure)

  is displayed. Press any key (except ENTRY OFF) to format drive B:.
- Switch off the SNA and remove the disk from drive A:. Then switch the instrument on again.
- Insert the disk containing the back-up of the RAM disk into drive A: of the SNA.
- Press <ALT>+ <F10> simultaneously to switch back to DOS mode. Press <RETURN> to display the DOS prompt C:\>.
- Use the external keyboard to enter the DOS command XCOPY A:*.* B:\ /e and then press RETURN. The entire contents of drive A: including all subdirectories will be copied to the RAM disk drive B:.
  The mesage "Overwrite B:\ <Filename> (Yes/NO/All) may appear on the display. Each time this happens, enter <N> <RETURN> to continue the process.

This completes restoration of the files to the SNA. Switch the instrument off, remove the disk from drive A: and switch on again. The user setups and the compensation data are now stored in the RAM drive.

4.10 Connecting an External Keyboard to the SNA

The SNA is fitted with a jack for connecting an external MF-2 keyboard (on the front panel of the instrument; EXT. KEYB, [1]). An external keyboard is useful or is required for running the SETUP program and service programs and when using the instrument in DOS mode.
The default keyboard driver loaded with the instrument software is for a US standard keyboard. This means that if a non-US keyboard is used, some keys may not have the expected functions.

4.10.1 Loading a Country-Specific Keyboard Driver

The external and built-in keyboards use the same keyboard driver.
The default driver is for the US-standard keyboard. If a driver for a non-US keyboard is installed, the key functions of the built-in keyboard may not be as expected (different functions or not recognized).

Permanent installation of a country-specific keyboard driver

The US keyboard driver is defined in the file B:\AUTO2.bat by the command "set KEYBXX=us". This file is executed automatically during boot-up of the SNA (assuming drive B: is correctly recognized).
The DOS editor can be used to change the file B:\AUTO2.bat. With the SNA in DOS mode, enter EDIT. Refer to the DOS handbook for details of how to use the editor function.
The non-US driver can be permanently set by changing the line "set KEYBXX=us" to (e.g, for a German keyboard) "set KEYBXX=gr" (see figure 4-6 on page 4-18). The abbreviations for other keyboard drivers are found in the DOS handbook.

Note: Make a back-up copy of the file B:\AUTO2.bat before making any changes (see DOS handbook for details of how to do this).

Temporary installation of a country-specific keyboard driver

Another keyboard driver which will remain loaded until the instrument is switched off again can be installed in place of the US driver as follows (example is for a German keyboard):

- Switch on and wait until the measurement display appears on the SNA screen
- Press <ALT>+ <F10> simultaneously to switch back to DOS mode. Press <RETURN> to display the DOS prompt C:\>.
- Type **<kezb gr>** and press RETURN to load the German driver. (The display shows [keyb gr] as the positions of the letters z and y on the US and German keyboards are reversed). The abbreviations for other keyboard drivers are found in the DOS handbook (note that the positions of some keys may be different!).

Note: The US keyboard driver is always loaded for the SETUP program for the AT CPU. It is not possible to load a different driver for operating this program.

```
@echo off
rem ---------------------------------------------------------------------------
rem ª This file is executed when the SNA boots up.
rem ª User-specific commands may be entered.
rem ---------------------------------------------------------------------------

rem ---------------------------------------------------------------------------
rem Parameter for DOS command MODE.
rem Settings also apply to hard copy output via
rem the serial interface.
rem ---------------------------------------------------------------------------
set PCOM1=com1:96,n,8,1
set PCOM2=com2:96,n,8,1

rem ---------------------------------------------------------------------------
rem KEYBXX sets the country-specific keyboard code XX.
rem "keyb XX" is set on boot up.
rem ---------------------------------------------------------------------------
set KEYBXX=us                "set KEYBXX=gr" for German keyboard
                             "set KEYBXX=us" for US keyboard

rem ---------------------------------------------------------------------------
rem CALOUT=1: CAL OUT can be switched on/off in the SPECTRUM/CAL menu
rem CALOUT= : CAL OUT isonly switched on during calibration
rem ---------------------------------------------------------------------------
set CALOUT=

rem ---------------------------------------------------------------------------
rem NOAUTOCAL=1: AUTO CAL is set to OFF on power-up
rem NOAUTOCAL= : AUTO CAL is set to ON on power-up
rem ---------------------------------------------------------------------------
set NOAUTOCAL=

rem ---------------------------------------------------------------------------
rem INIT_RST=1: USER MEM displays a menu for generating a Preset
rem               and Restart Setup ( writes the files
rem             %dlw%\sna\setups\s_*.000 and %dlw%\sna\setups\rst\s_*.000)
rem INIT_RST= : No menu for Preset Setup
rem ---------------------------------------------------------------------------
set INIT_RST=

rem ---------------------------------------------------------------------------
rem AUTO sets the procedure after this file has been executed.
rem AUTO=weiter: SNA software is started
rem AUTO=ende:   Help screen is displayed
rem AUTO=stop: No further action
rem ---------------------------------------------------------------------------
set AUTO=weiter

rem SY- AND ZF-DSP MUST BE LOADED FIRST (MEMORY SPACE)
rem set sy=noboot
rem set zf=noboot
rem zfdnam=sna\dzc_scw
rem ---------------------------------------------------------------------------
```

Fig. 4-6 Changes can be made to B:\AUTO2.bat to permanently install another keyboard driver

4.11 Switching from Instrument Software to DOS Mode and Vice-Versa

When the instrument is in measurement mode, pressing <ALT>+<F10> simultaneously on the external keyboard switches from the instrument software to DOS mode.
To revert to the instrument software, enter <k> and press the ENTER key.
You can also switch to DOS mode from the MODE menu. Press the MODE key and then press the DOS-UTILITIES softkey. Now press <ALT>+ <F1> simultaneously on the external keyboard to switch to DOS mode. Type <EXIT> press the ENTER key on the external keyboard to revet to the instrument software (in the DOS-UTILITIES menu item).

5 Fault Localization to Subassembly Level

5.1 Initial Fault Localization when a Measurement Error Occurs

The first step is to localize the fault to one of the following subassemblies. To do this, perform the checks detailed in the following chapters.

Checking the power supply output voltages	-> chapter 5.2
Checking the synthesizer function	-> chapter 5.6.2 and chapter 5.6.3
Checking internal and external calibration sources	-> chapter 5.5
Checking the frequency converter (input section)	-> chapter 5.3.1 and chapter 5.3.2
Checking the IF measurement unit	-> chapter 5.4

5.2 Checking the Power Supply Output Voltages

All power supply output voltages can be measured on the voltage distribution board [2101-BD] (fitted on top of the power supply); the values are given in the table below. The reference ground point is MT2 on board [2101-BD].

Test point on [2101-BD]	Value	Test point on [2101-BD]	Value
MT1	+5 V	B15	+12 V
MT3	+5 V	ST1.4	-21 V
B1	+6.8 V	ST1.8	+12 V
B2	+23 V	ST12.3	+5 V *
B8	-6.8 V	ST12.4	+15 V*
B10	+18 V	ST6.3	-18 V*
B11	-12 V		

Table 5-1 Test points for checking the power supply output voltages
*) These voltages are generated on board [2101-BD].

If one of the output voltages from the power supply is incorrect, the power supply should be replaced. Further troubleshooting of the power supply is not covered by this service manual. If one of the voltages generated on the voltage distribution board [2101-B] is incorrect, the circuit diagram can be used for further troubleshooting.

5.3 Fault Localization in the Frequency Converter (Input Section)

5.3.1 Checking the Attenuator (ATTN) Settings

First check whether a level error is present in all attenuator (ATTN) settings.

To check the attenuator, connect a level generator to the measurement input of the device under test (d.u.t) and make the following settings.

Instrument settings

D.U.T. (SNA-23):	
MODE	SPECTRUM ANALYSIS (CW)
FCENT	e.g. 10 MHz
FSPAN	10 kHz
RUN	SWEEP
REFERENCE	-30 dBm
RBW	1 kHz
ATTN	10 dB
Level generator:	
F	same as FCENT of D.U.T.
L	-30 dBm (50 Ω)

The measurement signal is first displayed on the reference line of the D.U.T. Next check all attenuator settings by changing the ATTN settings. The level display must remain the same for all ATTN settings. If the level changes, the attenuator is faulty.

5.3.2 Checking the Level in all Receive Bands

First check whether a level error is present in all bands.

To do this, connect a level generator to the measurement input of the D.U.T. and a spectrum analyzer to the IF output of the 422 MHz/22 MHz converter, 6BU2.

Instrument settings

D.U.T.:	
MODE	SPECTRUM ANALYSIS (CW)
FCENT	see table
FSPAN	0 Hz
RUN	HOLD or MAN
REFERENCE	0 dBm
RBW	10 MHz
ATTN	40 dB
Level generator:	
F	same as FCENT of D.U.T.
L	0 dBm (50 Ω)
Spectrum analyzer:	
MODE	SPECTRUM ANALYSIS (CW)
FCENT	21.99 MHz
FSPAN	5 MHz
REFERENCE	-30 dBm/1 dB/DIV (SCALE 10 dB)

Measure the level at the IF output of the 422 MHz/22 MHz converter (6BU2) using the spectrum analyzer in accordance with table 5-5.

D.U.T. (FCENT)	Value at 6BU2	Value at [60] *
22 MHz (Band 0)	-30 dBm	-10 dBm
3.3 GHz (Band 1)	-35 dBm (-38 dBm)	-11 dBm (-14 dBm)
13 GHz (Band 2)	-35 dBm (-38 dBm)	-11 dBm (-14 dBm)
21 GHz (Band 3)	-35 dBm (-38 dBm)	-11 dBm (-14 dBm)

Table 5-2 Table of levels for checking the frequency converter (input section)
Values in brackets apply to Series A + B instruments

Important: The column marked (*) contains the measured values after the IF selection. A measurement at this point can be made easily, since the test point is socket [60] on the instrument back panel. If a level error is detected here, the measurement should be repeated at 6BU2 to exclude the possibility of the fault being in the IF selection.

If an error is detected in the test, further troubleshooting in the frequency converter is described in chapter 5.3 on page 5-2.

5.3.3 Further Fault Localization Using the Level Diagram

Further fault localization can be done using the level diagram, figure 5-1 on page 5-5. The corresponding level and frequency values are given in table 5-3 on page 5-6 and table 5-4 on page 5-6. The level values are approximate and may vary by up to 3 dB.

Explanatory notes on the level tables

D.U.T. settings:

FCENT	see table (Band 0 = 10 MHz; Band 1 = 3.3 GHz)
FSPAN	0
INPUT ATTN	10 dB
SWEEP	HOLD or MAN

Level generator settings:

FCENT	see table (Band 0 = 10 MHz; Band 1 = 3.3 GHz)
FSPAN	0
SEND LEVEL	-30 dBm (50 Ω)

Connect the level generator to the input of the SNA and check the level values as per table 5-3 and table 5-4. All levels should be measured using a spectrum analyzer (50 Ω) directly, without a probe, by breaking the signal path (unless otherwise stated).

The level values given are approximate. Deviations from the values stated do not affect the accuracy of the D.U.T. as the level differences are calculated out by the internal and external calibration. Level deviations are only significant if the D.U.T. indicates incorrect levels despite internal and external calibration having been performed.

Caution!

If the fault is localized to a microwave module, the entire module and associated control circuit must be replaced. The microwave modules must not be opened. Opening these modules invalidates the guarantee, and the module can no longer be repaired in the factory.

Note: The coaxial SMA connectors for the microwave assemblies must be tightened to the specified torque value using the torque wrench specified in chapter 1.

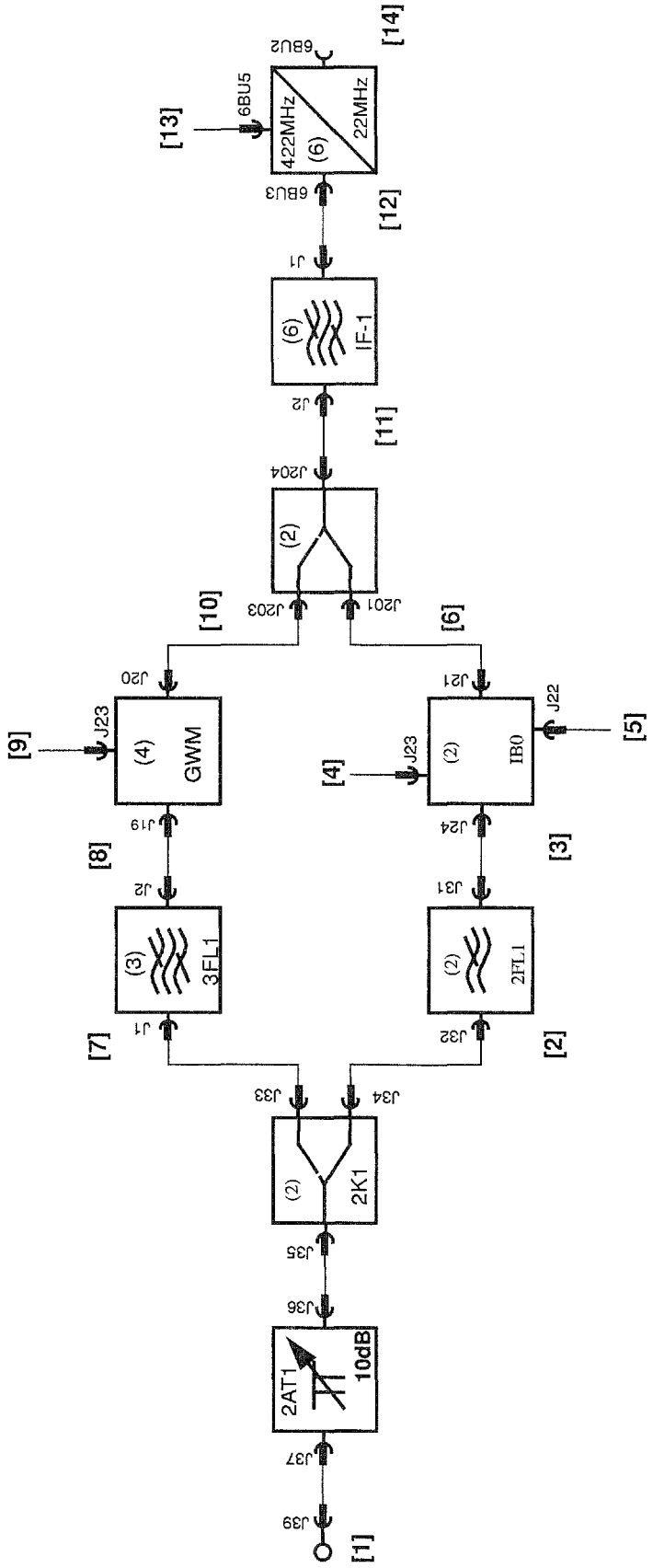


Fig. 5-1 Test points for the frequency converter level tables

Test point [ ] (see fig. 5-1)	Band 0		Band 1	
	Level	Frequency	Level	Frequency
1	-30 dBm	10 MHz	-30 dBm	3.3 GHz
2	-40 dBm	10 MHz	-	-
3	-40 dBm	10 MHz	-	-
4	+18 dBm	4.432 GHz	-	-
5	-2 dBm	400 MHz	-	-
6	-42 dBm	422 MHz	-	-
7	-	-	-41 dBm	3.3 GHz
8	-	-	-48 dBm	3.3 GHz
9	+15 dBm	4.432 GHz	+15 dBm	3.722 GHz
BU [71] 1st LO out	> +10 dBm	4.432 GHz	> +10 dBm	3.722 GHz
10	-	-	-58 dBm	422 MHz
11	-33 dBm	422 MHz	-41 dBm	422 MHz
12	-35 dBm	422 MHz	-43 dBm	422 MHz
13 *	+15 dBm	20 MHz	+15 dBm	20 MHz
14	-30 dBm	22 MHz	-38 dBm	22 MHz

Table 5-3 Level table for series A und B instruments
* high-impedance measurement using TK-10

Test point [ ]	Band 0		Band 1	
	Level	Frequency	Level	Frequency
1	-30 dBm	10 MHz	-30 dBm	3.3 GHz
2	-40 dBm	10 MHz	-	-
3	-40 dBm	10 MHz	-	-
4	+18 dBm	4.432 GHz	-	-
5	-2 dBm	400 MHz	-	-
6	-42 dBm	422 MHz	-	-
7	-	-	-42 dBm	3.3 GHz
8	-	-	-48 dBm	3.3 GHz
9	+15 dBm	4.432 GHz	+15 dBm	3.722 GHz
BU [71] 1st LO out	> +10 dBm	4.432 GHz	> +10 dBm	3.722 GHz
10	-	-	-58 dBm	422 MHz
11	-33 dBm	422 MHz	-38dBm	422 MHz

Table 5-4 Level table for instruments from series C onwards
* high-impedance measurement using TK-10

Test point [ ]	Band 0		Band 1	
	Level	Frequency	Level	Frequency
12	-35 dBm	422 MHz	-40 dBm	422 MHz
13*	+15 dBm	20 MHz	+15 dBm	20 MHz
14	-30 dBm	22 MHz	-35 dBm	22 MHz

Table 5-4 Level table for instruments from series C onwards
* high-impedance measurement using TK-10

5.4 Fault Localization in the IF Measurement Unit

5.4.1 Manual Check of the IF Measurement Unit

To check the IF measurement unit manually, connect a level generator to the measurement input of the D.U.T. Connect a spectrum analyzer to the IF output of the 422 MHz/22 MHz converter, 6BU2, and make the following instrument settings:

D.U.T.

MODE	SPECTRUM ANALYSIS (CW)
FCENT	Frequency in Band 0 (e.g. 10 MHz)
FSPAN	0 Hz
RUN	HOLD or MAN
REFERENCE	0 dBm
RBW	10 MHz
ATTN	40 dB

Level generator:

F	same as FCENT of D.U.T.
L	0dBm (50 Ω)

Spectrum analyzer:

MODE	SPECTRUM ANALYSIS (CW)
FCENT	21.99 MHz
FSPAN	5 MHz
REFERENCE	-30 dBm/1 dB/DIV (SCALE 10 dB)

Use the spectrum analyzer to measure the level at the IF output of the 422 MHz/22 MHz converter (6BU2).

With the above settings, the level at the input of the IF selection (7) BU1 should be - 30 dBm (reference level for the following measurements). To check the level within the IF measurement unit subassembly, check the signal path as per table 5-5.

Test point	Value	Notes
(7)BU1, (6)BU2	-30 dBm	IF selection input level, f = 21.99 MHz
(7)BU4, [60]	-10 dBm	IF selection test output. Switch the selection filter (RBW) between LC, crystal and bypass paths. The level at the test output should be practically the same for all signal paths.
(7)TP14, (7)BU3	-7 dB	IF selection output. High-impedance measurement using test probe. Test points (TP14, BU3) are DC coupled.
(8) TP24	4.5 to 5V	Logarithmizer output (DC). This voltage must also be present when the D.U.T settings remain the same and +5 dBm (50 Ω) is fed into the input of the logarithmizer (8)BU1.
(9) ST/BU 9, [63]	4.5 to 5V	Y output, same voltage as at (8)TP24. This is the analog input voltage for both the AD converters on the IF converter board. The voltage should be practically the same for all video filter (VBW) settings.

Table 5-5 Level table for checking the signal path in the IF measurement unitl

Important: With the settings stated above, the measurement line should be displayed on the top line of the display graticule if there is no fault present. The D.U.T. measurement line is, however, not indicative of the magnitude of the analog measurement signal, because the result of internal calibration is taken into account mathematically when displaying the value, i.e. the instrument display shows the mathematically corrected combination of the digitized value and the digitized result of internal calibration. This correction using calibration data is performed by the measurement unit controller.

5.5 Checking Internal and External Calibration Sources

The calibration source cannot be switched on permanently via the measurement software menus. It can be switched on permanently using the following procedure.

Switching on the cal source: Connect an external keyboard to the SNA. Switch the SNA on and wait until the measurement display appears. Now press <ALT> + <F10> simultaneously (SNA switches to DOS mode). Using the external keyboard, type "SET CALOUT=1" and press RETURN. (Entering "SET CALOUT=1" changes the CAL menu when the measurement software is re-started). Now type "K" to re-start the SNA measurement software. Select AUTO CAL OFF in the CAL menu of the D.U.T. The calibration source can now be switched on or off using the same menu (CAL. OUTPUT: ACTIVE/INACTIVE).

Important: If an internal calibration is triggered by changing a parameter (e.g. RBW, FCENT, etc.), the calibration source will be switched off afterwards and must be activated again from the CAL menu of the SNA. For this reason, AUTO CAL OFF mode should be set to avoid having to reactivate the source every time a parameter change is made.

Switching the instrument off resets the CAL menu to the original form (CAL. OUTPUT: ACTIVE/ INACTIVE is deleted from the menu).

Checking the external calibration source

Connect a precision level meter (50 Ω) to the external cal. output (socket [11] on front panel) of the D.U.T. The output level must be exactly -30 dBm (50 Ω) and the output frequency exactly 21.99 MHz.

Checking the internal calibration source

Connect a precision level meter (50 Ω) to the cal. output (11 BU13) for internal calibration of the D.U.T. The output level must be exactly -30 dBm (50 Ω) and the output frequency exactly 21.99 MHz.

Important: This method is not suitable for checking the guaranteed error limits of the calibration source as the level meter is not normally accurate enough. Exact checking of the calibration level specification can be done using the method suggested in the chapter "Checking the Specifications".

5.6 Fault Localization in the Synthesizer

5.6.1 General Information

The synthesizer generates the first local oscillator (carrier) frequency (1st LO), the other carrier frequencies and various clock signals.
A general check of the function of the synthesizer can be made by measurements at the 1st LO output (socket [71], back panel). The 1st LO frequency depends on the receive frequency selected (FCENT for FSPAN = 0). Calculation of the 1st LO frequency for receive frequencies in all receive bands is indicated in chapter 5.6.3.

5.6.2 Checking the 10 MHz Reference Frequency

Use a spectrum analyzer (e.g. SNA-7, SNA-23/33) to check the 10 MHz output signal at BU13 [64] on the D.U.T. back panel.

5.6.3 Checking the 1st LO Frequency

Connect a spectrum analyzer, e.g. SNA-7, SNA-23/33 to the 1st LO output socket [71] of the D.U.T. Synchronize the D.U.T. externally to the 10 MHz from the SNA-7/23 via socket 10 [62]. Set the D.U.T. to FSPAN = 0 and FCENT as per the following table. set the D.U.T. to MANUAL (Sweep Mode [RUN] = MAN).

Measure the frequency and level of the 1st LO for each setting.
The level should be **> +10 dBm** for each frequency setting.

FCENT (D.U.T.)	1st LO frequency
2.5 GHz (Band 0)	6.92199 GHz
5.5 GHz (Band 1)	5.92199 GHz
13 GHz (Band 2)	6.710995 GHz
21 GHz (Band 3)	5.3554975 GHz

Table 5-6 Table for checking the synthesizer (1st LO)

If a fault is detected in this test, localize the fault further within the synthesizer module using the instructions in chapter 5.6 on page 5-10.

Relationship between the synthesizer frequency (1st LO) and the receive frequency (RF)

The 1st LO frequency depends on the selected receive frequency (FCENT for FSPAN = 0). The complete frequency range of the SNA-23 from 0 Hz to 30 GHz is split into four frequency bands (Band 0 to Band 3). The 1st LO frequency (synthesizer output) is used to convert the RF signal to the IF (421.99 MHz). The LO frequency is used directly for conversion in frequency bands 0 and 1. In band 2, the LO frequency is first doubled; in band 3, it is quadrupled. Multiplication of the 1st LO is performed by the "Fundamental Mixer" microwave module.
The 1st LO can be calculated in each frequency band using the following relationships. The frequency limits for the various receive bands are shown in table 5-7.

Band 0: 1st LO = RF +IF1 (4.42199 GHz)

Example: The SNA is tuned to a receive frequency of 2.5 GHz (FCENT). The frequency span (FSPAN) is 0 Hz. The synthesizer output frequency (1st LO) will then be:

1st LO = 2.5 GHz +4.42199 GHz = 6.92199 GHz

Band 1: 1st LO = RF + IF2 (421.99 MHz)

Example: The SNA is tuned to a receive frequency of 5.5 GHz (FCENT). The frequency span (FSPAN) is 0 Hz. The synthesizer output frequency (1st LO) will then be:

1st LO = 5.5 GHz +421.99 MHz = 5.92199 GHz

Band 2: $1st\ LO = \frac{RF + IF2\ (421.99\ MHz)}{2}$

Example: The SNA is tuned to a receive frequency of 13 GHz (FCENT). The frequency span (FSPAN) is 0 Hz. The synthesizer output frequency (1st LO) will then be:

1st LO = (13 GHz +421.99 MHz) : 2 = 6.710995 GHz

Band 3: $1st\ LO = \frac{RF + IF2\ (421.99\ MHz)}{4}$

Example: The SNA is tuned to a receive frequency of 21 GHz (FCENT). The frequency span (FSPAN) is 0 Hz. The synthesizer output frequency (1st LO) will then be:

1st LO = (21 GHz +421.99 MHz) : 4 = 5.3554975 GHz

Band limits and corresponding LO frequencies for SNA-23

The complete frequency range of the SNA-23 from 0 Hz to 30 GHz is split into four frequency bands (Band 0 to Band 3). The table below shows the exact frequency limits for these bands and the synthesizer LO frequencies for these bands.

Band	Frequency range(FCENT, FSPAN = 0)		Synthesizer output frequency (1st LO)
0	0 Hz	to 3.199 999 999 GHz	4.421 990 000 GHz to 7.621 989 999 GHz
1	3.2 GHz	to 7.499 999 999 GHz	3.621 990 000 GHz to 7.921 989 999 GHz
3	7.5 GHz	to 14.999 999 999 GHz	3.960 995 000 GHz to 7.710 995 000 GHz
0	15 GHz	to 30 GHz	3.855 497 500 GHz to 7.605 497 500 GHz

Table 5-7 Band limits and corresponding synthesizer output frequencies (1st LO)

5.7 Fault Localization in the Controller

The controller core is an AT CPU. The operating system used is MS-DOS. A knowledge of this operating system is assumed in the following . The DOS handbook is very useful for interpreting the messages and commands.

If a fault is suspected in the controller, start troubleshooting in the AT CPU.

5.7.1 Procedure when a Fault is Suspected in the Controller

- Switch on the SNA (make sure there is no disk in drive A:)
- Compare the instrument behavior with the normal boot up behavior described in chapter 4.1.
- Check the settings in the CMOS setup (see chapter 4.5)
- If the instrument does not boot the operating system when switched on, try to boot it from a bootable disk (see chapter 4.3)
- If error messages are displayed after the operating system and instrument software have loaded, or if the instrument software is aborted due to an error (2101 Debug Output is displayed), evaluate the error messages as indicated in chapter 4.4.

6 Fault Localization to Component Level

6.1 Fault Localization in the Frequency Converter

6.1.1 Information on the Frequency Response Correction for Bands 0, 1, 2 and 3

If any module in the signal path from the input socket [12] through to (6)J2 including all waveguides is repaired or replaced, adjustment of the frequency response is necessary.

A special test setup is used to determine the frequency response correction values during "adjustment". Compensation tables are generated and stored in the SNA for each of the receive bands (0, 1, 2 and 3). The values in the tables are then applied to the measured values during normal operation of the SNA to give the correct display values.
Recording the frequency response correction values requires a complex computer-controlled test setup and can only be performed by service centers specially equipped for this task.

> ***Caution!***
> If a fault is located in a microwave module, the entire module and associated control circuit should be replaced. The microwave module should not be opened. Opening the modules invalidates the guarantee and such modules can no longer be repaired in the factory.

Troubleshooting within the microwave modules is therefore not covered by this service manual. Chapter 5 describes fault localization to defective microwave modules. If the fault is in the control circuit for the module, a repair may be possible in exceptional cases. Normally, the entire module, complete with control circuit, should be replaced.

6.1.2 Integration Band 0 Control [2101-CF]

Error signals F1 and F2 are generated by the microwave module "Integration Band 0". The error signals are not evaluated by the instrument software; they can be checked on the Integration Band 0 Control board using an oscilloscope. Use the circuit diagram as an aid to troubleshooting and check the DC working points first.

DC working points (voltages at test points and connectors)

U_J6 and U_J7	+5.0 V ± 50 mV		
U_J8 and U_J9	-3.6 V		
U_J4	+11 V		
U_J5	-2.5 V to -1.5 V	if Band 0 ON;	(MP1.8: 5 V)
	-0.4 V to 0 V	if Band 0 OFF;	(MP1.8: 0 V)
U_J10	+10.7 V		

Error signal F1

The +5 V supply voltage for the hybrid working point regulator (J6, J7) is current-limited. This voltage is also compared with a reference voltage at the same time. If the voltage drops below the reference, error signal F1 is generated (HIGH to MP10.9).

Error signal F1 may be due to the following:

- Current drain on the +5 V supply too high
- +12 V, -12 V, +6.5 V operating voltages missing

Error signal F2

A check is made that the VCO is locked. If the VCO is not locked, error signal F2 is generated (HIGH to MP10.10).

Error signal F2 may be due to the following:

- 400 MHz signal to socket J22 missing
- Supply voltage (J10) for 400 MHz amplifier missing
- +18 V, +12 V, -12 V operating voltages missing
- Beat frequency at TP1 >15 MHz (offset range too high). Once it is certain that there is no error in the RF circuit and that none of the above faults is present, R54 must be re-adjusted, as described in section 7.6.2 on page 7-15.

The PLL circuit can assume four states:

- I VCO locked, normal operating state
- II VCO not locked and offset range <15 MHz, search oscillator oscillating at approx. 80 Hz, VCO locks within about 20 ms.
- III VCO not locked, offset range approx. 15 to 20 MHz, search oscillator oscillating, VCO cannot lock because voltage span of tuning voltage is max ± 0.6 V.
- IV VCO not locked, offset range >20 MHz, search oscillator off as offset range too high.

6.1.3 YIG Filter 3FL1 and YIG Filter Control

Introduction

The YIG filter characteristic is determined individually and stored in Flash ROM on the YIG filter controller.
Recording the YIG filter characteristic requires complex computer-controlled equipment and can therefore only be performed in service centers specially equipped for this purpose.

If the YIG filter or the YIG filter controller is replaced, the YIG filter characteristic must be recorded and stored for the new components (see section 7.5.3).

6.1.3.1 YIG Filter Control [2101-AS1]

Checking the power supply

Measure the following voltages on circuit board [2101-AS1] using a DVM:

Test point	Value	Notes
U46, Pin1	+24 V	Operating voltages for (1)ST6 (PSU / Voltage distribution)
R1	+23 V	
R79	+5 V	
R75	-18 V	
Voltages "generated" on-board		
Q4 (emitter)	+15 V	
Q5 (emitter)	-15 V	
U42 Pin7	+7 V (V-Ref)	DAC reference voltage
Voltage drop across R74	approx. 220 mV	YIG heater current , approx . 220 mV (ca. 100 mA) when YIG thermally stable.

Table 6-1 YIG filter controller [2101-AS1] operating and supply voltages

Checking the function of the YIG filter controller

The basic function of the controller is checked by measuring the current through the YIG filter at various frequency settings. To do this, open the connection J21/P21 (MCX plug) and insert an ammeter in series with the YIG filter. Set the D.U.T. to FSTART = 3.2 GHz and FSTOP = 30 GHz. Manually tune the SNA to various frequencies in the range 3.2 to 30 GHz. A certain current, dependent on the frequency setting, must flow through the YIG filter; this value should increase continuously as the frequency increases. Typical values of YIG current for a given YIG frequency are shown in table 6-2.

Important: The current increase is not necessarily linear, as it depends on the YIG characteristic which is determined during adjustment (see section 7). The correction values are programmed into the Flash ROM on the YIG filter controller board during adjustment. The measured values (FCENT, current through YIG filter) may thus differ from the values in the table, but a continual increase in the current with increasing frequency must be measurable.

FCENT	Current through YIG filter	FCENT	Current through YIG filter
3.2 GHz	95 mA	16 GHz	480 mA
4 GHz	120 mA	18 GHz	540 mA
4.5 GHz	135 mA	20 GHz	600 mA
6 GHz	180 mA	22 GHz	660 mA
8 GHz	240 mA	24 GHz	720 mA
10 GHz	300 mA	26 GHz	785 mA
12 GHz	360 mA	28 GHz	845 mA
14 GHz	420 mA	30 GHz	905 mA

Table 6-2 Typical YIG frequency / YIG current values

If no increase in current can be measured for increasing frequencies, there is a fault in the YIG controller or in the interfaces to the input section controller (control, frequency band information) or to the synthesizer (frequency information).

Checking the interface to the synthesizer

The synthesizer frequency information can be checked against table 6-3. Set the D.U.T. to FSPAN = 0 (MAN Tuning) and to the frequencies (FCENT) in the table. If the frequency information is correct, the signals given in the table will be present at U1 and U2 of the YIG filter controller board [2101-AS1].

Test point	FCENT			Signal name
	2 MHz	15 GHz	29.662 GHz	
U1 PIN2	1	1	1	FS(0)
U1 PIN3	0	0	1	FS(1)
U1 PIN4	0	0	1	FS(2)
U1 PIN5	0	0	1	FS(3)
U1 PIN6	0	0	1	FS(4)
U1 PIN7	0	1	1	FS(5)
U1 PIN8	0	1	1	FS(6)
U1 PIN9	0	1	0	FS(7)
U2 PIN2	0	1	0	FS(8)
U2 PIN3	0	1	1	FS(9)
U2 PIN4	0	1	1	FS(10)
U2 PIN5	0	0	1	FS(11)
U2 PIN6	0	1	0	FS(12)
U2 PIN7	0	1	1	FS(13)
U2 PIN8	0	0	1	FS(14)
U2 PIN9	0	0	0	FS(15)

Table 6-3 Table for checking the synthesizer frequency information

If the signals do not correspond to the table, there is a fault in the synthesizer controller board [2101-A] in the area of the YTF-PORT.

6.1.3.2 Checking the YIG Filter

Once the tests above have been made, the pass-band characteristic of the YIG filter in its built-in state can be checked. This check assumes correct function of the YIG filter controller.

Connect a sweepable RF generator to the input of the D.U.T. and set the instruments as follows:

D.U.T.

FCENT:	5.5 GHz (any frequency above 3.2 GHz)
FSPAN:	120 MHz
REFERENCE:	= TX level of generator
SCALE:	50 dB
SWT	100 s

Generator

FCENT:	5.5 GHz (any frequency above 3.2 GHz)
FSPAN:	120 MHz
SWT:	0.5 s (or smallest possible value)

First tune the D.U.T.to FCENT (5.5 GHz) (FSPAN = 0) and set switch 3S2 on the YIG filter controller board to YIG Hold. This locks the YIG filter at the previously set frequency (5.5 GHz) even if the input frequency to the D.U.T. is changed.
Set the SPAN to 120 MHz again, and sweep the D.U.T. slowly. If the controller is working properly, the pass-band of the YIG filter will be shown on the display. A typical pass band characteristic is shown in fig. 6-1.

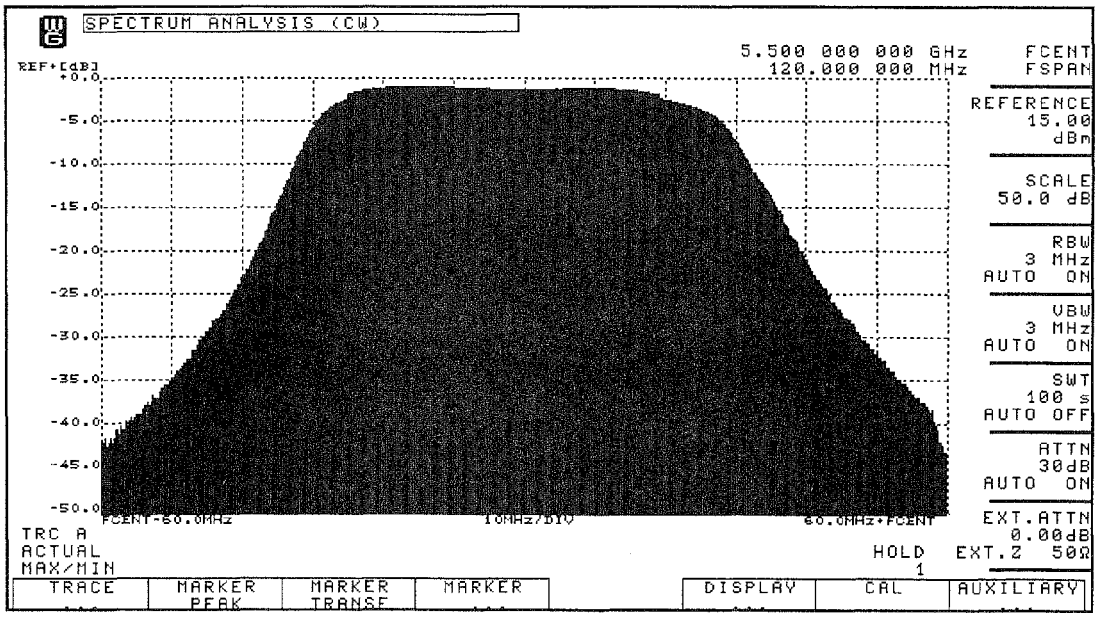


Fig. 6-1 Typical pass-band characteristic of YIG filter 3FL1

If the YIG filter is faulty, it must be replaced. Frequency response correction is required after replacing the YIG filter (see "Information on the Frequency Response Correction for Bands 0, 1, 2 and 3" on page 6-1).

6.1.4 Fundamental Mixer Controller [2101-AV1]

The error signal is generated on the fundamental mixer controller. It is not evaluated by the instrument software but can be checked with an oscilloscope at MP2.4; ERROR SIGNAL on the fundamental mixer controller board.

Error signal

The error signal may be due to the following causes:

- Current drain on +5 V voltage too high
- +6.5 V operating voltage missing
- +12 V operating voltage missing
- -12 V operating voltage missing

DC working points (voltages at the test points and plug connectors)

U_TP1	+ 9.3 V
U_TP2	- 9.3 V
U_J1, U_J2, U_J3	+ 5.0 V ± 50 mV
U_J6	- 3.5 V

Band switching control signals

The band switching control signals can be checked against table 6-4. Set the D.U.T. to FSPAN = 0 and set FCENT to a frequency in the band required. Band ranges are listed in table 6-5.

Band	TP6	TP7	J9	J10	J11	J12	J13	J14
0	L	L	1	1	0	1	1	0
1	H	L	0	1	1	1	0	1
2	L	H	0	1	0	0	1	1
3	H	H	1	0	1	0	1	1

Table 6-4 Band switching control signals on the fundamental mixer controller board

L : 0 V
H : 5 V
0 : negative voltage: approx. -6 V to -10 V, depending on control pin
1 : positive voltage: approx. 10 V

Note: Remove the fundamental mixer from its fixing plate to access the test points.

Band	Start of band	End of band
0	0 Hz	3.199999999 GHz
1	3.2 GHz	7.499999999 GHz
2	7.5 GHz	14.999999999 GHz
3	15.0 GHz	26.5 GHz (30 GHz)

Table 6-5 SNA-23 frequency band limits

6.1.5 IF Switch [2101-AQ1]

Checking the supply voltages

The operating voltages for the IF switch module [2101-AQ1] are derived from the input section controller board (5). Check the voltages against the table below.

Test point	Value
C245	+12 V
C244	-12 V

Table 6-6 IF switch [2101-AQ1] operating voltages

Checking the drive signals

The IF switch allows one of the three inputs (421.99 MHz IF level) to be switched through to the output (J204)The three input signals are fed into the MCX sockets (J201, J202 and J203).

- J201: Input signal fed from "Band 0 frequency converter" microwave module, when the SNA is tuned to a frequency in Band 0 (RF 0 to 3.199 GHz).
- J203: Input signal fed from "Fundamental mixer" microwave module, when the SNA is tuned to a frequency in Band 1,2 or 3 (RF 3.2 GHz to 30 GHz).
- J202: Input signal fed from socket [70] "IF-INPUT". This input is selected when the SNA is in SPECTRUM ANALYSIS (EXT MIXER) mode.
- J204: IF switch output.

Check the IF switch control signals against the following table:

Setting	Test point		Notes
	C243	C242	
Band 0	1	0	Insrument tuned in Band 0, IF switch input J201 selected
Band 1 ... 3	0	0	Insrument tuned in Band 1,2 or 3, IF switch input J203 selected
EXT MIXER	0	1	SPECTRUM ANALYSIS (EXT MIXER) mode set, IF switch input J202 selected (= BU 70 on instrument back panel)

Table 6-7 IF switch [2101-AQ1] control signals

Checking the signal paths

Use a network analyzer, e.g. SNA-62 to measure the gain of the three signal paths at 421.99 MHz. Normalize the SNA-62 (short circuit) before each measurement. The SNA-62 input is connected to J204 (output) of the IF switch.

Important: The gain values quoted for the three paths are approximate; the actual values may differ (by approx. ± 2 dB) without a fault being present. Level matching has been carried out in this module to cope with the scatter in component values between different series of the instrument. A much larger difference in the level is to be expected if there is a fault, so that this method can be used to check for a faulty IF switch.

Band 0 signal path

Set the SNA-62 TX level to -42 dBm (50 Ω) and connect the generator output to input J201 of the IF switch. Set the D.U.T. to a frequency in Band 0 (e.g. FCENT 100MHz, FSPAN 0). Read off the gain on the SNA-62.

Nominal value: Gain +9 dB

Band 1, 2 and 3 signal path

Set the SNA-62 TX level to -58 dBm (50 Ω) and connect the generator output to input J203 of the IF switch. Set the D.U.T. to a frequency in Band 1,2 or 3 (e.g. FCENT 10 GHz, FSPAN 0). Read off the gain on the SNA-62.

Nominal value:	Gain +16 dB	(Series A + B)
	Gain +19 dB	(Series C onward)

External mixer signal path

Set the SNA-62 TX level to -30 dBm (50 Ω) and connect the generator output to input J202 of the IF switch (or Bu 70 on the back panel). Set the D.U.T. to SPECTRUM ANALYSIS (EXT MIXER) mode. Read off the gain on the SNA-62.

Nominal value:	Gain +16 dB	(Series A + B)
	Gain +19 dB	(Series C onward)

If the gains of the three signal paths differ significantly from these values, the IF switch chould be replaced.

6.1.6 Input Section Control [2101-AR]

Attenuator drive

The settings of switches S2.2, 2.3 and 2.4 select a control table for driving the attenuator (ATTN) as determined by the setting made. The switch settings are scanned by the PIO module (5)U11 and the control words corresponding to the selected control table are output for controlling the attenuator from this same module (Port 3).
To check the attenuator drive, the settings of switches S2.4, S2.3 and S2.2 must first be determined. These settings determine the control table (see table 6-8). The table lists all attenuator types which have been used up till now.

S2.4	S2.3	S2.2	Attenuator (Range/Steps/ Frequency range)	Control table no.
0	0	0	65 dB/5 dB/26.5 GHz (Weinschel 5690-1)	1
0	0	1	70 dB/10 dB/40. 27 GHz (W&G FED-5/02, HP 33321 G/K)	2
0	1	0	70 dB/5 dB/4 GHz (W&G FED-5/01)	3
0	1	1	70 dB/10 dB/4 GHz (Weinschel 151-70)	4
1	0	0	Not used	-

Table 6-8 Control table for selecting various types of attenuator (control table no.)

Once the correct control table has been established, the attenuator drive can be checked against one of the tables below. Set the input attenuator (ATTN) to the values stated and check the control words at the stated test points using an oscilloscope.

Note: The control words shown in the control tables can only be measured during the switching phase of the attenuator, as the attenuator relays are bistable. In the idle state, all test points are HIGH ("1").

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
0	1	1	1	1	0	0	0	0
5	1	1	1	0	0	0	0	1
10	1	1	0	1	0	0	1	0
15	1	1	0	0	0	0	1	1
20	1	0	1	1	0	1	0	0
25	1	0	1	0	0	1	0	1
30	1	0	0	1	0	1	1	0
35	1	0	0	0	1	1	1	1
40	0	1	0	1	1	0	1	0
45	0	1	0	0	1	0	1	1
50	0	0	1	1	1	1	0	0

Table 6-9 Control table no.1

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
55	0	0	1	0	1	1	0	1
60	0	0	0	1	1	1	1	0
65	0	0	0	0	1	1	1	1

Table 6-9 Control table no.1

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
0	1	1	1	1	0	0	0	0
10	1	1	1	0	0	0	0	1
20	0	1	1	1	1	0	0	0
30	0	1	1	0	1	0	0	1
40	0	0	1	1	0	1	0	0
50	0	0	1	0	1	1	0	1
60	0	0	0	1	1	1	1	0
70	0	0	0	0	1	1	1	1

Table 6-10 Control table no.2

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
0	1	1	1	1	0	0	0	0
5	1	0	1	1	0	1	0	0
10	1	1	1	0	0	0	0	1
15	1	0	1	0	0	1	0	1
20	0	1	1	1	1	0	0	0
25	0	0	1	1	1	1	0	0
30	0	1	1	0	1	0	0	1
35	1	1	0	1	0	0	1	0
40	1	0	0	1	0	1	1	0
45	1	1	0	0	0	0	1	1
50	1	0	0	0	0	1	1	1
55	0	1	0	1	1	0	1	0

Table 6-11 Control table no.3

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
60	0	0	0	1	1	1	1	0
65	0	1	0	0	1	0	1	1
70	0	0	0	0	1	1	1	1

Table 6-11 Control table no.3

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
0	X	1	1	1	X	0	0	0
10	X	1	1	0	X	0	0	1
20	X	0	1	1	X	1	0	0
30	X	0	1	0	X	1	0	1
40	X	1	0	1	X	0	1	0
50	X	1	0	0	X	0	1	1
60	X	0	0	1	X	1	1	0
70	X	0	0	0	X	1	1	1

Table 6-12 Control table no.4 (X = no significance)

Checking the EXT mixer bias current

Switch (5) S2.10 must be closed (BIAS ON setting). Unsolder the connection to (2) C241 (IF_U\Bias EXM) and connect an ammeter (digital multimeter, range ± 20 mA DC) between (2) C241 and the unsoldered cable. Set the D.U.T. to SPECTRUM ANALYSIS (EXT MIXER) mode.

Set the "DC-Bias" to 12.8 mA (SPECTRUM ANALYSIS (EXT MIXER) menu) and compare with the display on the digital multimeter.

Nominal value: 12.8 mA ± 0.05 mA

Set the "DC-Bias" in the external mixer menu to 0 mA and compare with the display on the digital multimeter.

Nominal value: 0 mA ± 0.05 mA

6.1.7 Interdigital Filter (6IF1)

The interdigital filter can be checked with a network analyzer (e.g. SNA-62). The settings for the SNA-62 are shown in fig. 6-2. Make these settings and then normalize the SNA-62. Connect the SNA-62 generator output to the filter input (J1) and the filter output (J2) to the SNA-62 input.

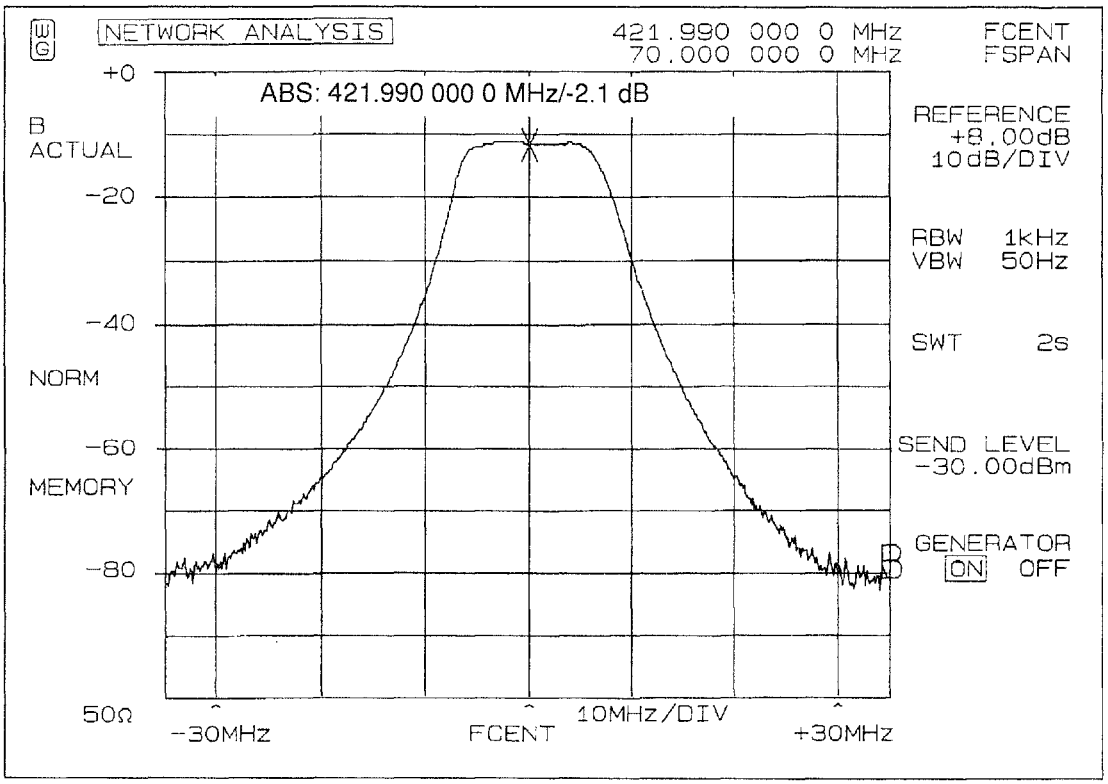


Fig. 6-2 Typical pass-band characteristic for interdigital filter 6IF1

The insertion loss of the interdigital filter at f_0 (422 MHz) should not exceed 2.5 dB. The attenuation minimum must be at exactly 422 MHz (421.99 MHz). If these values are not obtained (particularly the minimum at 422 MHz), the filter should be replaced. Do not attempt to adjust the filter, as special equipment is required for this.

6.1.8 422 MHz/22 MHz Converter [2101-X]

Checking the power supply

Measure the following voltages with a DVM:

Test point	Nominal value
TP 2.1	10.5 V ± 0.2 V
TP 2.2	5.2 V ± 0.2 V
TP 1.3	-10.0 V ± 0.2 V
C 13	5.0 V ± 0.1 V

Table 6-13 422 MHz/22 MHz converter [2101-X] power supplies

If the nominal values are not met, use the circuit diagram to troubleshoot.

Checking the 400 MHz carrier generator

Measure the following voltages with a DVM:

Test point	Nominal value
IC 5.2	3.0 V ± 0.2 V
GL 4	6.5 V ± 0.5 V

Table 6-14 400 MHz carrier generator

If the nominal values are not met, there is a fault in the frequency generator.

Set the D.U.T. to SPECTRUM ANALYSIS (CW) and measure the level of the 400 MHz carrier using a probe (with 1:10 divider) and a spectrum analyzer as in the following table.

Test point	Nominal value
IC 9.4	+19 dBm ± 1 dB (50 Ohm)
R 57	+ 9 dBm ± 1 dB (50 Ohm)
T 8.E	+12 dBm ± 1 dB (50 Ohm)

Table 6-15 Frequency generator test points

Remember to take the 20 dB attenuation of the 1:10 divider into account.
The frequency may be between about 380 MHz and 420 MHz if the frequency generator is faulty.

If the carrier level and frequencies are correct, further troubleshooting as under "Checking the 422 MHz/22 MHz converter signal path" on page 6-16.

Checking the 400 MHz oscillator

Open the regulator loop by unsoldering **(6) R 26** and feed an external control voltage from a PSU to (6) R 26 - R 25.
If the oscillator still does not oscillate, troubleshoot using the circuit diagram and check the following working points:

Test point	Nominal value
C 67	9.7 V
C 27	9.5 V
C 22	9.5 V
C 47	9.5 V
C 37	4.8 V

Table 6-16 Typical working points for checking the 400 MHz oscillator

If the oscillator oscillates when the external control voltage is applied, measure the frequency at (6) IC 9.4 using a probe (with 1:10 divider) and a spectrum analyzer. Alter the control voltage from the PSU as per the table and compare the frequencies with the values in the table.

Control voltage	Frequency
0 V	377 MHz
2 V	383 MHz
4 V	388 MHz
6 V	396 MHz
8 V	405 MHz
10 V	415 MHz
12 V	425 MHz

Table 6-17 Typical frequency values as a function of control voltage

Checking the frequency divider (400 MHz)

Set the control voltage from the PSU so that the oscillator runs at approx. 400 MHz. Measure the following signals with an oscilloscope (see fig. 6-3).

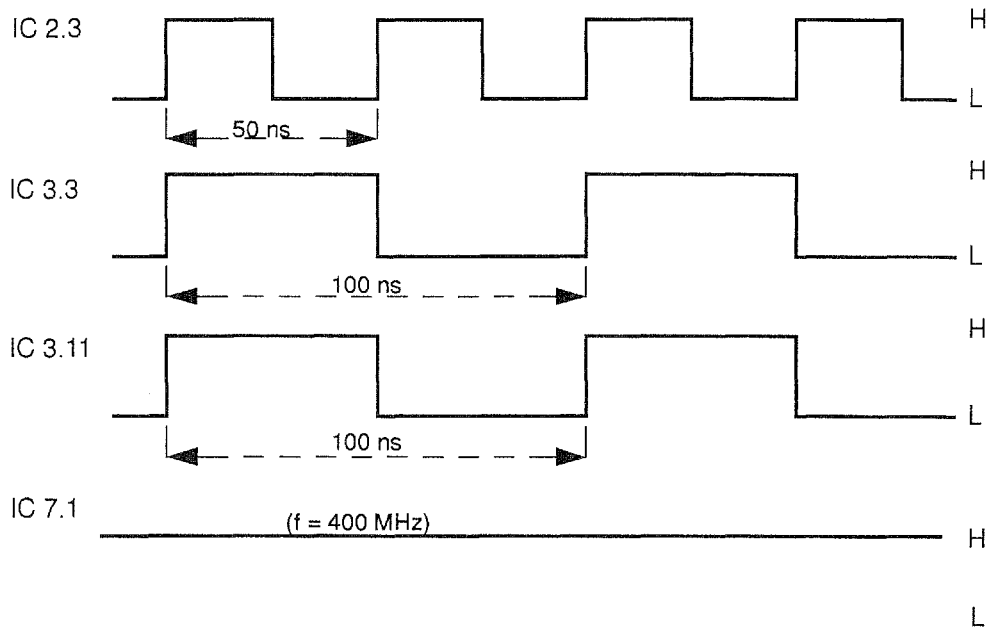


Fig. 6-3 Test points for checking the 40:1 divider (L = 0 V, H = 5 V)

If the oscillograms look different, troubleshoot using the circuit diagrams.

Checking the phase meter (400 MHz)

Set the control voltage from the PSU so that the oscillator runs at approx. 390 MHz. Measure the following signals with an oscilloscope (L = 0 V, H = 5 V):

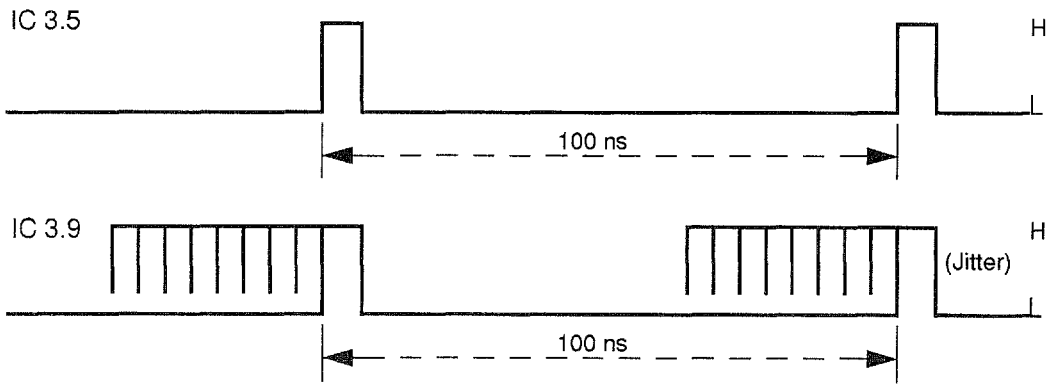


Fig. 6-4 Oscillograms for checking the phase meter

Set the control voltage from the PSU so that the oscillator runs at approx. 410 MHz. Measure the following signals with an oscilloscope (L = 0 V, H = 5 V):

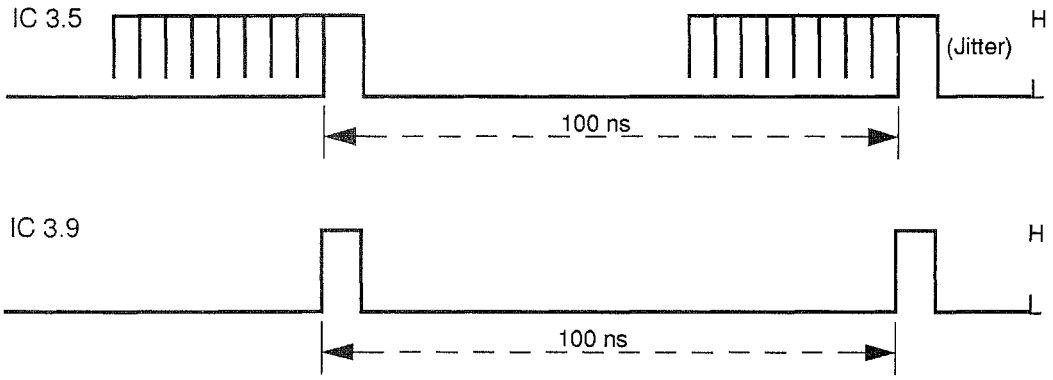


Fig. 6-5 Oszillogramme zur Überprüfung des Phasenmessers

If the oscillograms look different, troubleshoot using the circuit diagrams.

Note: Solder (6) R 26 back in place after the measurements.

Checking the 422 MHz/22 MHz converter signal path

Checking the DC working points in the signal path

Measure the following DC working points using a DVM:

Test point	Nominal value
IC 8.3	5.5 V ± 0.5 V
IC 13.3	5.5 V ± 0.5 V
IC 14.3	4.4 V ± 0.2 V

Table 6-18 Signal path DC working points

If the nominal values are not met, troubleshoot using the circuit diagrams.

Signal path level check

Connect a level generator to the input of the D.U.T.

D.U.T.: SPECTRUM ANALYSIS (CW)
FCENT 22 MHz
FSPAN 0 Hz, (RUN MAN)
REFERENCE 0 dBm
ATTN 40 dB

Level generator: 22 MHz, 0 dBm (50 Ω)

Measure the signal level using a probe and a spectrum analyzer (see table 6-19).
Measure the 400 MHz carrier level at IC9.4 using a probe (with 1:10 divider) and a spectrum analyzer (see table 6-15 on page 6-13).

Test point	Frequency	Nominal value
R 102	421.99 MHz	-40 dBm ± 1 dB (50 Ω)
R 103	421.99 MHz	-42 dBm ± 1 dB (50 Ω)
R 65	421.99 MHz	-30 dBm ± 1 dB (50 Ω)
R 64	421.99 MHz	-33 dBm ± 1 dB (50 Ω)
R 60	21.99 MHz	-40 dBm ± 1 dB (50 Ω)
R 59	21.99 MHz	-43 dBm ± 1 dB (50 Ω)
R 11	21.99 MHz	-31 dBm ± 1 dB (50 Ω)
R 114	21.99 MHz	-29 dBm ± 1 dB (50 Ω)

Table 6-19 Signal path levels

If the nominal values are not met, troubleshoot using the circuit diagrams.

6.2 Troubleshooting the IF measurement section

6.2.1 IF selection [2101-L]

Function check

Bu4 on the IF selection board leads to the external IF output Bu10 [60] on the back panel. The function of the IF selection can thus be checked without opening the instrument
Feed a level of -30 dBm (50 Ω) into the D.U.T input, socket [12] eingespeist. Set the D.U.T. to the frequency of the generator (FCENT = TX frequency, e.g. 20 MHz; FSPAN = 0 Hz; RUN MAN). The D.U.T. REFERENCE is also set to -30 dBm gesetzt. At a D.U.T. resolution bandwidth (RBW) of 10 MHz (bypass path), the signal at Bu4 or Bu10 [60] on the back panel should be -10 dBm, F = 21.99 MHz when terminated with Ra = 50 Ω.
The level result should be approximately the same for RBWs of 3 MHz, 1 MHz, 300 kHz, 100 kHz, 30 kHz, 10 kHz and 1 kHz.

If there is a level error during the above check, a manual measurement can be used for troubleshooting:

Measurement of operating voltages

TP16:	+12 V	(I ≤ 0.2 A)
TP18:	-12 V	(I ≤ 0.2 A)
TP17:	+5 V	(4.75 V to 5.45 V)
TP19:	-5 V	(-4.75 V to -5.45 V)
TP15:	-10 V	(-9.16 V to -10.86 V. Inverted reference voltage from GI400 for DAC)
TP10:	-7.8 V	(-7.15 V to -9.0 V, reference voltage for amplifier stages V2 to V5 referred to +5 V.

Measuring the signal path level (without selection filter)

Feed a level of approx. -30 dBm (f = 21.99 MHz) into the IF selection input socket (7BU1) and set the D.U.T. as follows:

FCENT	21.99 MHz
FSPAN	0 Hz (RUN MAN)
SCALE	10 dB
RBW	10 MHz (bypass path, no selection filter active)
VBW	10 MHz
INPUTT ATTN	0 dB
REFERENCE	-27 dBm
AUTO CAL	OFF

Close wire link 17.1 - 18 on the IF selection board. This drives IF selection amplifier stage V1 with maximum gain, v = 6 to 7.5 dB (v = 1 with wire link open).

This setting switches the following signal path on the IF selection board:

Input:	7BU1
Pre-attenuator 0/-14 dB:	0 dB
Amplifier V1:	maximum (v = 6 to 7.5 dB)
Filter path:	bypass (no LC or crystal filter switched in)
Amplifier V2	0 dB
Attenuator 0/-2 dB	0 dB
Amplifier V3	0 dB

Attenuator 0/-1 dB	0 dB
Amplifier V4	0 dB
Amplifier V5	0 dB

Use a level meter or spectrum analyzer to troubleshoot by measuring the level as per table 6-20 with a high-impedance probe (e.g. TK-10).

> ***Caution!***
> Some test points are DC coupled, so always use a test probe.

Test point	Level	Notes
Bu1	-39 dB	Reference level f = 21.99 MHz
C 14	- 39dB	Pre-attenuator 0 dB
Pin 1 von V1	- 26 dB	Input V1; gain T2/UE2 ca. 13 dB
TP 3	- 19 dB	Output V1; gain V1 = max
Pin 1 von V2	- 19 dB	Input V2
TP 6	- 19 dB	Output V2; gain V2 = 0 dB
Pin 1 von V3	- 19 dB	Attenuator 0/-2 dB set to 0 dB
TP 7	- 19 dB	Output V3; gain V3 = 0 dB
Pin 1 von V4	- 19 dB	Attenuator 0/-1 dB set to 0 dB
TP 8	- 19 dB	Output V4; gain V4 = 0 dB
TP 9	-19 dB	Output V5; gain V5 = 0 dB
BU3; TP 14	-7 dB	Output amplifier gain approx. 12 dB

Table 6-20 IF selection level table

Checking the IF amplifier stages and pre-attenuator

After this, the individual attenuators and amplifier stages can be switched singly or together and their function checked by setting the D.U.T. REFERENCE as per table 6-21 on page 6-20. Measure the output level at 7BU3 (use high-impedance probe, test point is DC coupled) and reduce or increase the input level in accordance with the attenuator or amplifier setting (see table 6-21 on page 6-20). The output level at 7BU3 must remain constant (same as for reference measurement, input level -30 dBm and D.U.T. reference setting -27 dBm). The D.U.T. reference settings required for full checking of the IF amplifier stages are shown in bold type in the table. The input signal to 7Bu1 required for these settings is also shown in the table.

Important: The pre-attenuator 0/-14 dB and amplifier V3 (0/-16 dB) cannot be activated singly. With the check method used, combinations of amplifiers are switched in such cases (reference settings -23 dBm and -56 dBm). If a fault occurs at these settings, all other amplifier stages and attenuators which can be switched singly should be checked first. A defective stage can thus be isolated.

Reference D.U.T.	Pre-attenuator 0/-14 dB	V2 0/16 dB	0/-2 dB	V3 0/16 dB	0/-1 dB	V4 0/8 dB	V5 0/4 dB	Input level at 7Bu1
-23 dBm	**1**	0	**1**	0	0	**1**	**1**	-26 dBm
-24 dBm	0	0	1	0	1	0	0	
-25 dBm	0	0	**1**	0	0	0	0	-28 dBm
-26 dBm	0	0	0	0	**1**	0	0	-29 dBm
-27 dBm	0	0	0	0	0	0	0	-30 dBm (ref. level)
-28 dBm	0	0	1	0	1	0	1	
-29 dBm	0	0	1	0	0	0	1	
-30 dBm	0	0	0	0	1	0	1	
-31 dBm	0	0	0	0	0	0	**1**	-34 dBm
-32 dBm	0	0	1	0	1	1	0	
-33 dBm	0	0	1	0	0	1	0	
-34 dBm	0	0	0	0	1	1	0	
-35 dBm	0	0	0	0	0	**1**	0	-38 dBm
-36 dBm	0	0	1	0	1	1	1	
-37 dBm	0	0	1	0	0	1	1	
-38 dBm	0	0	0	0	1	1	1	
-39 dBm	0	0	0	0	0	1	1	
-40 dBm	0	1	1	0	1	0	0	
-41 dBm	0	1	1	0	0	0	0	
-42 dBm	0	1	0	0	1	0	0	
-43 dBm	0	**1**	0	0	0	0	0	-46 dBm
-44 dBm	0	1	1	0	1	0	1	
-45 dBm	0	1	1	0	0	0	1	
-46 dBm	0	1	0	0	1	0	1	
-47 dBm	0	1	0	0	0	0	1	
-48 dBm	0	1	1	0	1	1	0	
-49 dBm	0	1	1	0	0	1	0	
-50 dBm	0	1	0	0	1	1	0	
-51 dBm	0	1	0	0	0	1	0	

Table 6-21 Divider and gain settings as a function of the REFERENCE setting

Reference D.U.T.	Pre-attenuator 0/-14 dB	V2 0/16 dB	0/-2 dB	V3 0/16 dB	0/-1 dB	V4 0/8 dB	V5 0/4 dB	Input level at 7Bu1
-52 dBm	0	1	1	0	1	1	1	
-53 dBm	0	1	1	0	0	1	1	
-54 dBm	0	1	0	0	1	1	1	
-55 dBm	0	1	0	0	0	1	1	
-56 dBm	0	1	1	1	1	0	0	-59 dBm

Table 6-21 Divider and gain settings as a function of the REFERENCE setting

Checking the selection filter

The selection filter can be checked using the procedure in the section "Checking the Specifications" in this service manual. If a fault is detected during checking of the selection filter, troubleshoot using the circuit diagram and the adjustment instructions in section 7.7.1.

6.2.2 Logarithmizer [2101-M]

6.2.2.1 Operating and bias voltages

The voltages should be measured in the order given below unless there are good reasons for not doing so:

Supply voltages

TP16: +6.5 V ± 0.3 V
TP17: -6.5 V ± 0.3 V
TP18: +12 V ± 0.5 V
TP19: -11.9 V to -13 V

Important: The voltage at TP19 is critical. It must not be below 11.9 V.

Voltages generated on the circuit board

TP21: +5 V ± 50 mV
TP22: -5 V ± 50 mV

D to A converter reference voltage

TP20: +10.6 V to +11.0 V

Logarithmic amplifier working point

Measure between TP19 (-12 V operating voltage) and TP10.

$U_{(TP19-TP10)}$ 4 V ± 10 mV

Rectifier reference voltage

TP7: -5.05 V to -5.15 V

Reference voltage after the buffer amplifier

U(TP8) = U(TP7) ± 2 mV

Rectifier threshold voltage

Measure between TP8 and TP9

$U_{(TP8 - TP9)}$ 900 mV ± 1.5 mV

Rectifier current source voltage

The voltage at TP6 must be 5.8 V ± 10 mV below the voltage at TP8.

TP6 ≈ -10.9 V

6.2.2.2 Troubleshooting the logaritnmizer signal path

The logarithmizer signal path can be checked using a spectrum analyzer (e.g. SNA-3 with TK-11) or a selective level meter (e.g. SPM-19 with TK-11). All signals in the logarithmizer signal path are in the IF range of 21.99 MHz. The test points andpositions of the log. stages are shown in fig. 6-6.

A level of -40 dBm at a frequency of e.g. 10 MHz is fed into the input of the SNA-20/-23. The following settings are made on the D.U.T/:

D.U.T.: SPECTRUM ANALYSIS (CW)
FCENT 10 MHz (= frequency of feed signal)
FSPAN 0 Hz, (RUN MAN)
REFERENCE 30 dBm
SCALE 100 dB
RBW 1 kHz
ATTN 35 dB

Level generator: 10 MHz, -40 dBm (50 Ω)

The measured levels should be as given in table 6-22.

Test point	Value	Notes
(7) TP14	approx. - 60 dB	IF selection output level, f = 21.99 MHz, **= reference level**
TP 23,25	approx. -63 dB	Level after buffer stage, corresponds to log. stage 1 input level. The two test points are identical
Log. stage 1, Pin 3, 9	- 63 dB	Log. stage 1 input level
Log. stage 1, Pin 13, 21	- 53 dB	Log. stage 1 output level
Log. stage 2, Pin 3, 9	- 53 dB	Log. stage 2 input level
Log. stage 2, Pin 13, 21	- 43 dB	Log. stage 2 output level
Log. stage 3, Pin 3, 9	- 43 dB	Log. stage 3 input level
Log. stage 3, Pin 13, 21	- 33 dB	Log. stage 3 output level
Log. stage 4, Pin 3, 9	- 33 dB	Log. stage 4 input level
Log. stage 4, Pin 13, 21	- 23 dB	Log. stage 4 output level

Table 6-22 Level table for checking the logarithmizer signal path

Test point	Value	Notes
Log. stage 5, Pin 3, 9	- 23 dB	Log. stage 5 input level
Log. stage 5, Pin 13, 21	- 13 dB	Log. stage 5 output level
Log. stage 6, Pin 3, 9	- 13 dB	Log. stage 6 input level
Log. stage 6, Pin 13, 21	- 3 dB	Log. stage 6 output level (corresponds to noise filter input level)
Log. stage 7, Pin 3, 9	- 3 dB	Log. stage 7 output signal, signal after noise filter If the level at htis point is incorrect, check the noise filter
Reduce the level at the input of the D.U.T. by 30 dB		
Log. stage 7, Pin 3, 9	- 33 dB	Log. stage 7 input level
Log. stage 7, Pin 13, 21	- 23 dB	Log. stage 7 output level
Log. stage 8, Pin 3, 9	- 23 dB	Log. stage 8 input level
Log. stage 8, Pin 13, 21	- 13 dB	Log. stage 8 output level
Log. stage 9, Pin 3, 9	- 13 dB	Log. stage 9 input level
Log. stage 9, Pin 13, 21	- 3 dB	Log. stage 9 output level
Log. stage 10, Pin 3, 9	- 3 dB	Log. stage 10 input level
Log. stage 10, Pin 13, 21	+ 7dB	Log. stage 10 output level

Table 6-22 Level table for checking the logarithmizer signal path

Important: The above test checks only the signal path of the logarithmizer (10 x 10 dB log. amplifiers). A rectifier is connected after each log. stage; this converts the analog 21.99 MHz (AC) output signal form the amplifier into a DC signal. The above test does not check the function of the rectifiers (see circuit description, section 9). If the signal path is error-free, the rectifiers and the adder circuit should be checked.

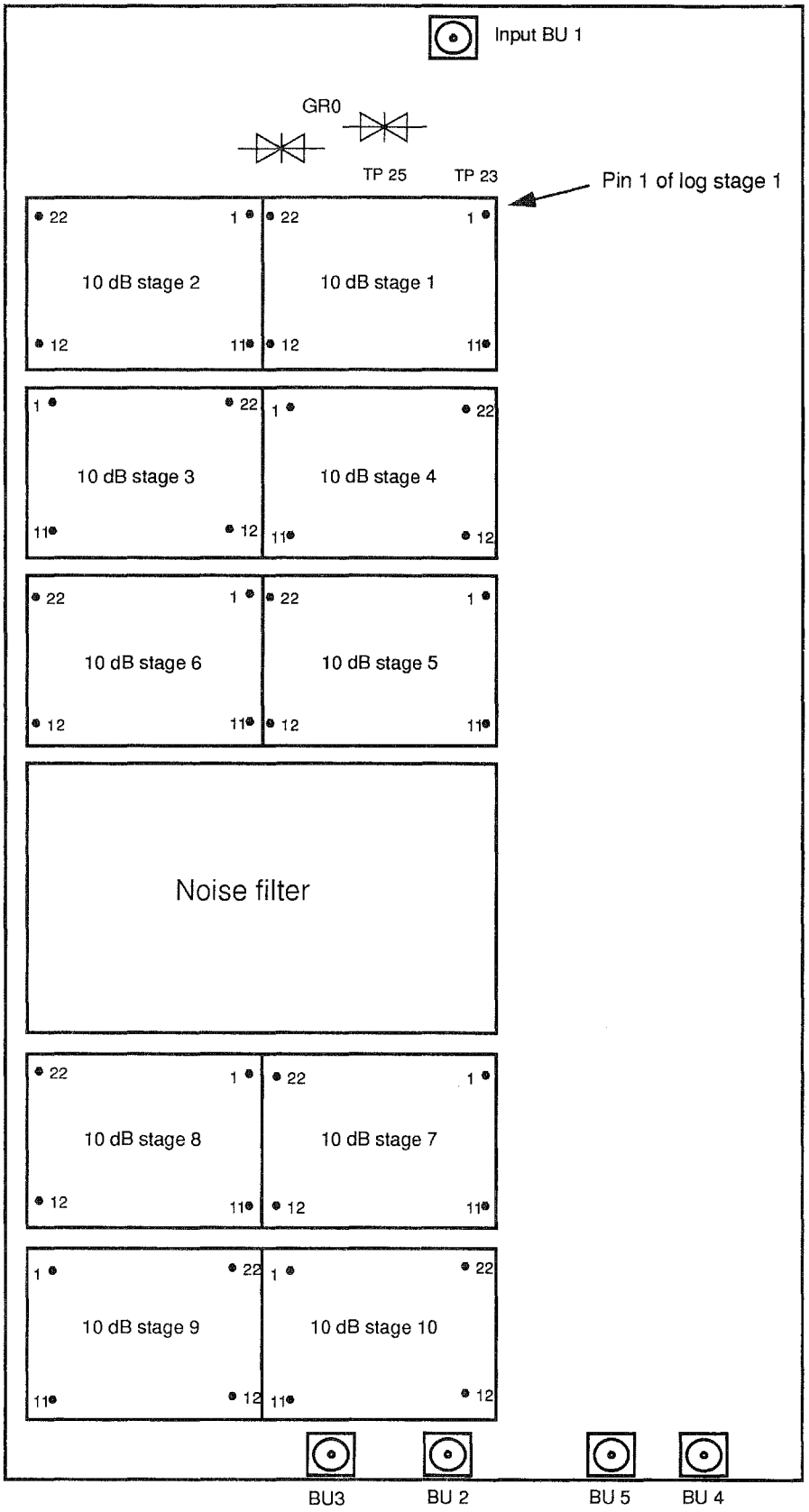


Fig. 6-6 Layout of log. stages and test points on the logarithmizer board (simplified diagram)

6.2.3 IF converter [2101-O] (series A +B)

Operating and bias voltages

The voltages should be measured in the order given below unless there are good reasons for not doing so:

Supply voltages

Voltage	Test point	Value	Tolerance	Notes
+12 V	TP5	+11.6 V	± 0.2 V	
-12 V	TP6	-11 V	± 0.2 V	
+6.5 V	TP7	+6.4 V	± 0.2 V	Only required for ADC
-6.5 V	TP8	-6.4 V	± 0.2 V	Only required for ADC
+5 V	TP4	+5 V	± 0.2 V	

Table 6-23 Supply voltages on the IF converter board

Checking the analog signal path

Unplug the plug from 9Bu1 (connection to logarithmizer) and feed a DC voltage of about 2.5 V into TP1.
If +2.5 V is fed in (check voltage at TP1), the following values apply for the signal path:

Test point	Value
IC2.2	+2.5 V
IC7.8	+2.5 V
IC13.6	+2.5 V
TP2	-1 V ± 50 mV
TP3	+2.5 V ± 50 mV

Table 6-24 Analog signal path test points on the IF converter board

Checking the 8-bit converter

The following signals must be present at the 8-bit converter (IC 16) for correct operation:

Test point	Value	Notes
IC16.17	20 MHz digital signal	Clock, HCMOS level
IC16.26	-2 V ± 50 mV	Reference voltage, derived from IC11, generated by IC12/T300
IC16.27	-1 V ± 50 mV	Center of reference voltage
IC16.12, 28	+5 V	+VCC, digital control signal for output format

Table 6-25 Signals at the IF converter 8-bit converter (IC 16)

Test point	Value	Notes
IC16.23	-1 V ± 50 mV	Analog input
IC16.6,10	+5 V ± 0.2 V	VCC
IC16.7,8,9	-5 V ± 0.2 V	VEE

Table 6-25 Signals at the IF converter 8-bit converter (IC 16)

Checking the 16-bit converter

The following signals must be present at the 16-bit converter (IC 20) for correct operation

Test point	Value	Notes
IC20.20	4 MHz digital signal	Main clock, HCMOS level
IC20.1	40 kHz digital signal	Converter clock, HCMOS level
IC20.28	+5 V ± 50 mV	Reference voltage generated by IC19, derived from the 8-bit ADC reference voltage
IC20.29	+5 V ± 50 mV	Reference output, same as IC20.28
IC20.26	2.5 V	Analog input
IC20.11	+5 V ± 0.2 V	VCC digital
IC20.25	+5 V ± 0.2 V	VCC analog
IC20.36	-5 V ± 0.2 V	VEE digital
IC20.30	- 5V ± 0.2 V	VEE analog
IC20.37	40 kHz digital signal	End of track
IC20.39		Serial clock; 16 x 1 MHz clock pulses every 25 µs (40 kHz)
IC20.40		Serial data
IC20.21..24,32..35		Digital control inputs. The measurement mode states are:
IC20.21	H	
IC20.22	H	
IC20.23	H	
IC20.24	L	
IC20.32	L	
IC20.33	H	
IC20.34	H	
IC20.35	L	

Table 6-26 Signals at the IF converter 16-bit converter (IC 20)

Checking the RMS rectifier

The RMS rectifier is tested with a DC voltage. Unplug the plug from 9Bu1 (connection to logarithmizer) and feed a DC voltage of about 2.5 V into TP1. If +2.5 V is fed in (check voltage at TP1), the following values can be measured with a voltmeter:

Test point	Value
IC9.6	0.35 to 0.45 V
IC10.7	-0.75 to -0.7 V
IC8.7	2.5 V (same as TP1, ± 10 mV
IC15.2	0.35 to 0.45 V
IC15.6	1.3 to 1.4 V
IC8.2	2.7 to 2.8 V
IC8.1	5.5 to 6.5 V
IC10.2	0.35 to 0.45 V

Table 6-27 Test points for checking the RMS amplifier

6.2.4 IF converter [2101-O] (series C onwards)

The 8-bit converter (IC 16) is replaced by a 10-bit converter (IC 16) in instruments from series C onwards. There are some minor changes in the circuit compared with series A + B; these are unimportant for troubleshooting. The same procedure can be used as described under "Checking the 8-bit converter" on page 6-25 in section 6.2.3.

6.2.5 Calibration generator [2101-N]

The following instructions are for a rapid, systematic check. For precise checking of the calibration level, refer to section 7.7.4 ("Calibration generator (11)[2101-N]").

Operating voltages

Check the operating voltages for the calibration generator board against the following table:

Test point	Value	Notes
TP14	+12 V	If one of these voltages is missing, check the AC PSU
TP18	-12 V	
TP16	+6.5 V	
TP19	-6.5 V	
TP20	+5V	Voltage looped-through to measurement unit controller, not used by calibration generator
TP17	+5V	Voltages "generated" on-board. Check the area around IC40, T400, T401, GL401 if there is a fault.
TP15	+10 V	

Table 6-28 Operating and supply voltages on the calibration generator board

Checking the calibration synthesizer (PLL)

Test point	Value	Notes
TP4	20 MHz	Reference frequency, HCMOS level
TP3	1.818 MHz	Reference frequency divided by 11. If this frequency is missing, check IC7. Check that : P0 = 0, P1 = 1, P2 = 1, P3 = 0; in the event of a fault, IC8 is not initialized correctly, check the computer bus.

Table 6-29 Table for checking the calibration synthesizers

Checking the VCO

The calibration generator must be switched on to check the VCO (GL101 off, anode at 0).

The calibration source cannot be permanently activated from the software menu. The following procedure should be used:

Activating the calibration source: Connect an external keyboard to the SNA. Switch on and wait for the measurement screen to appear. Then press <ALT> and <F10> simultaneously (SNA switches to DOS mode). Enter "SET CALOUT=1" from the keyboard and press return to confirm. Now enter "K" followed by return to re-start the SNA measurement program. Select AUTO CAL OFF in the CAL menu of the D.U.T. The calibration source can now be activated/ deactivated from this menu (CAL. OUTPUT: ACTIVE/INACTIVE).

Unplug the shorting link 1.2-1.3 and use it to close link 1.1-1.2 (U_{VCO} = 0 V):

Frequency at TP2: 40 to 42 MHz
at TP6: 20 to 21 MHz

Remove the shorting link completely (U_{VCO} = -12 V):

Frequency at TP2: 64 to 70 MHz
at TP6: 32 to 35 MHz

VCO slope

To check the VCO slope, remove shorting link (BR1) completely and remove R110 (otherwise TP1 is pulled down to -12 V. Feed the appropriate DC voltage (see table) in at TP1 and measure the VCO frequency. The following values must be obtained.

Frequency (TP6)	$U_{VCO} = U_{TP1}$
17 MHz	+2.2 V ± 0.2 V
20 MHz	+0.1 V ± 0.2 V
22 MHz	-1.2 V ± 0.2 V
24 MHz	-2.7 V ± 0.2 V
27 MHz	-5.0 V ± 0.3 V

Table 6-30 Table for checking the VCO slope

If no frequency can be measured at TP2, the oscillator is not running. Check the potentials at T100 to T102 and check transformer UE1 for short circuits.

Checking the level control

Unplug the shorting link from 2.1-2.2 and use it to link 2.2-2.3. This feeds the maximum level to the output (BU12, BU13). This level is approx.-23 dBm (50 Ω) if the board has been adjusted.

Under the above condition, the following DC working points apply (see table 6-31).

Test point	Value	Notes
IC20.8	-9.2 V	**Note:** The "pip" on IC20 indicates pin 12
IC20.9	-10.0 V	
IC20.4,7	-6.2 V	
IC20.5,6	-1.0 V	
IC20.2	-5.7 V	All voltages are approximate (± 0.2 V)
IC20.3	-6.5 V	
IC20.1,10	-5.2 V	
IC20.11,12	-4.0 V	
GL200	-6.4 V	± 0.5 V

Table 6-31 Table for checking the level control

Checking the FM demodulator

Feed a stable frequency, e.g. 10 MHz from instrument back panel, into the SNA input. Set the SNA as follows:

FCENT 10 MHz
FSPAN 5 MHz
RBW 3 MHz
SEEP(RUN) MAN TUNING

First set f = FCENT and check the demodulator input signal at TP11:
f = 21.99 MHz
u = approx. 200 mV_{pp}

The signal should be 2 V_{pp} at IC 31.1 and 4 with a phase difference between the signals of 180.

Check the DC voltage levels at IC31 against the following table:

Test point	Value
IC31.8,10	+4V
IC31.5	-10.5 V
IC31.6,12	+8.2 V ± 0.3 V

Table 6-32 DC voltage levels at IC31

Connect a DVM to TP12 (= IC31.12). Stepwise increase in the frequency (manual tuning) by 10 kHz should increase the voltage by approx. 200 mV for each step. Reducing the frequency should result in voltage drop.

Final values (approx.):

12 MHz: 11.1 V
8 MHz: 4.8 V

6.3 Troubleshooting the controller

6.3.1 AT CPU

This service manual does not support troubleshooting of the AT CPU to component level. We do not recommend repairing this board, due to the complex SMD chip set components.
The AT CPU runs a self-test of its computer core immediately after switch on (BIOS TEST, see section 4). If a fault in the AT CPU is detected during this test, the module should be replaced. Special PC test programs, such as "Checkit" can be used for further checking. These provide comprehensive tests for the interfaces, RAM and other CPU peripherals. Such programs are available from PC accessory shops.

6.3.2 Memory [2101-AF] (series A - E)

Supply voltages

The supply voltages are fed from the interface board via 3 50-way ribbon cables(P1,P2 and P3).

The following voltages must be present on the memory board:

Test point	Value	Notes
e.g. D701 (anode)	+5 V	+5 V ± 5%; I = 400 mA
Q701 (emitter)	+12 V	+12 V ± 5%; I = 60 mA Program voltage for Flash-ROMs

Table 6-33 Memory board [2101-AF] operating voltages

Effects of memory board errors

Error during BIOS test (e.g. test aborted)

As the memory is directly connected to the AT bus, a fault on the board can affect data and address communications via the bus (bus conflict).

To check whether the memory board is the cause of a bus conflict, decouple the memory board from the bus system by setting the control signal "NDOE" = HIGH. This is done by removing (17)U203. The memory board then only passes the bus from the AT CPU to the interface board and provides the supply voltage for the AT CPU.

Important: If (17)U203 is removed to prevent the AT CPU from accessing the memory board, the operating system and instrument software will not be loaded when the instrument is switched on. Prepare a system disk (operating system) beforehand. The instrument can also be booted from the service disk.

Operating system/instrument software does not load

If the operating system system and/or the instrument software is not loaded after switching on but the BIOS test is completed successfully, a fault on the memory board (17) is likely, since both the operating system and the instrument software are stored in the Flash-ROMs on this board.

To determine which of the Flash components is defective, the instrument software should be re-programmed into the Flash-ROMs (see "Installing the Instrument Software / Updating Software" on page 4-14). If an error occurs during deletion and re-programming, the program indicates the

address which caused the error. Use table 6-34 to determine the pair of Flash ROMs (16-bit data) for the given address. It is not possible to determine which of the two Flash ROMs thus identified is faulty.

Important: The addresses are assigned to different components, depending on whether 1 Mbit or 2 Mbit Flash ROMs are fitted.

Hexadecimal address	Memory type	Components
580 000 - 5BF FFF	SRAM, battery-buffered	U300, U303, U205, U207
5C0 000 - 5FF FFF	SRAM, battery-buffered	U301, U304, U205, U207
920 000 - 920 3FF	Flash ROM VPP control signal	U204
921 800 - 921 8FF	Memory status port control signal	U204
When fitted with 1 Mbit memory components:		
940 000 - 97F FFF	Flash; correction value memory	U512, U513, U205, U207
C80 000 - CBF FFF	Flash; program memory	U510, U511, U205, U207
CC0 000 - CFF FFF	Flash; program memory	U508, U509, U205, U207
D00 000 - D3F FFF	Flash; program memory	U506, U507, U205, U207
D40 000 - D7F FFF	Flash; program memory	U504, U505, U205, U207
D80 000 - DBF FFF	Flash; program memory	U502, U503, U205, U207
DC0 000 - DFF FFF	Flash; program memory	U500 U501, U205, U207
E00 000 - E3F FFF	Flash; program memory	U412, U413, U205, U207
E40 000 - E7F FFF	Flash; program memory	U410, U411, U205, U207
E80 000 - EBF FFF	Flash; program memory	U408, U409, U206, U208
EC0 000 - EFF FFF	Flash; program memory	U406, U407, U206, U208
F00 000 - F3F FFF	Flash; program memory	U404, U405, U206, U208
F40 000 - F7F FFF	Flash; program memory	U402, U403, U206, U208
F80 000 - FBF FFF	Flash; program memory	U400, U401, U206, U208
0E0 000 - 0EF FFF	Flash; extended BIOS	U400, U401, U206, U208
When fitted with 2 Mbit memory components:		
940 000 - 9BF FFF	Flash; correction value memory	U512, U513, U205, U207
9C0 000 - A3F FFF	Flash; program memory	U508, U509, U205, U207
A40 000 - ABF FFF	Flash; program memory	U506, U507, U205, U207
AC0 000 - B3F FFF	Flash; program memory	U504, U505, U205, U207
B40 000 - BBF FFF	Flash; program memory	U502, U503, U205, U207
BC0 000 - C3F FFF	Flash; program memory	U500 U501, U205, U207
C40 000 - CBF FFF	Flash; program memory	U412, U413, U205, U207
CC0 000 - D3F FFF	Flash; program memory	U410, U411, U205, U207
D40 000 - DBF FFF	Flash; program memory	U408, U409, U206, U208
DC0 000 - E3F FFF	Flash; program memory	U406, U407, U206, U208

Table 6-34 Addresses and corresponding components on the memory board [2101-AF]

Hexadecimal address	Memory type	Components
E40 000 - EBF FFF	Flash; program memory	U404, U405, U206, U208
EC0 000 - F3F FFF	Flash; program memory	U402, U403, U206, U208
F40 000 - FBF FFF	Flash; program memory	U400, U401, U206, U208
0E0 000 - 0EF FFF	Flash; extended BIOS	U400, U401, U206, U208
Memory components U510 and U511 are not fitted		

Table 6-34 Addresses and corresponding components on the memory board [2101-AF]

Correction tables deleted after switching off

After switching on and booting of the operating system, the message

General failure reading drive B
Abort, Retry, Fail?

is displayed.

The memory board is fitted with 512 kByte of battery-buffered SRAM (U300, U301, U303 and U304) in which the correction data for the frequency response and logarithmizer are stored (see "Installation of compensation (correction) data" on page 7-11). Data loss can be caused by a defective memory component, a faulty battery (BT1) or a fault in U306 and its associated circuitry (Q300, R301, R302, R303).

Measure the following voltages with the instrument switched off:

Test point	Value	Notes
U306 Pin1	> 2.2 V	Battery voltage when connected up
TP308, U306 Pin 2	> 2.1 V	Instrument switched off. If faulty, test U306 and associated circuitry
U300,301,303,304 Pin 12	> 2.1 V	VCC1 for SRAM components 2.1 V - 3.7 V instrument switched off approx. 5 V instrument switched on
TP 309	HIGH	Status signal NLOW_BAT, LOW if battery voltage < 2.2 V

Table 6-35 Test points for checking the SRAM buffer voltage on the memory board

Error writing to Flash ROMs

If errors occur during write operations to the Flash ROMs, the program voltage "generated" on the board may be faulty. During delete and programming operations, 12 V ± 5% must be present on pin 1 of the Flash components. The same voltage must be present at the emitter of Q701. The SVPP signal (MP700) should also be checked.

SVPP (MP700) HIGH: Program voltage for Flash ROMs is on. VPROG = +12 V

SVPP (MP700) LOW: Program voltage for Flash ROMs is off. VPROG = +5 V

6.3.3 Keyboard [2101-AJ]

Supply voltages

The supply voltages are fed via ribbon cable (MT3) from the interface board via the keyboard controller board.

The following supply voltages can be measured on the keyboard:

Test point	Value	Notes	
e.g. IC1,IC3, IC4 Pin 20	+5 V	+5 V ± 5%	
MT3.6	+12 V	+12 V ± 5%	These voltages are not required on this board
MT3.8	-12 V	-12 V ± 5%	

Table 6-36 Power supply voltages for the keyboard [2101-AJ]

Faulty key

The control of the key matrix can be checked with an oscilloscope connected to the outputs of IC2. Individual rows are driven cyclically with a LOW signal. Check the inputs of IC1 to see if pressing a key generates the corresponding LOW signal at the input of IC1 for the row being driven.

Faulty LED

The LED states can be measured at the outputs of IC3 and IC4. HIGH means that the LED should be onl The individual LEDs can be switched on and off by changing the operating mode. If the contents of latches IC3 and IC4 remain constant, the fault is in the latch drive, the data bus or in the latches themselves.

6.3.4 Keyboard controller [2101-AL]

Supply voltages

The supply voltages for the keyboard controller are derived from the interface board and fed in via ribbon cable (MT3).
The following voltages can be measured on the keyboard controller board:

Test point	Value	Notes	
ST6.3	+5 V	+5 V ± 5%	
ST6.5	+12 V	+12 V ± 5%	These voltages are not required on this board. They are fed to boards (20) and (21) via ST5.
ST6.7	-12 V	-12 V ± 5%	

Table 6-37 Supply voltages for the keyboard controller [2101-AL]

Keyboard controller function groups

The keyboard controller can be split into the following function groups for troubleshooting:

No.	Function group	Components in function group
1	Computer core	IC2, IC3, IC6, IC15.6, Q1
2	Built-in keyboard controller	IC8
3	External keyboard interface	IC13.1, IC13.2, IC13.5, IC13.6
4	Output to external keyboard	IC13.3, IC13.4, IC14.1, IC14.2
5	Input from external keyboard	IC7, IC8, IC9, IC10, IC11, IC12, IC14.3-5
6	Rotary control controller	IC7, IC8

Table 6-38 Keyboard controller function groups and their components

Fault location

Error message: "Keyboard error"

If this error message is displayed during boot-up, the fault is likely to be in function group 1 or 3.

Internal keyboard does not work, external keyboard works properly

Function group 2 or keyboard printed circuit board is defective.

External keyboard does not respond

If the external keyboard LEDs do not respond, the fault is likely in function group 4.

External keyboard does not work, internal keyboard works properly

Function group 5 or external keyboard is defective.

Rotary control does not respond

Function group 1 or 6 is defective.

6.4 Troubleshooting the synthesizer OD-11

6.4.1 Standard frequency oscillator

The 10 MHz sinusoidal signal from the standard frequency oscillator ("10MHZRF") can be output to an oscilloscope from St101 Pin 9. The peak value is > 0.7 V. It is also present as a FACT signal at IC15. Signals synchronous with the standard frequency oscillator only appear at outputs "20MHZ_1" to "20MHZ_3" (50BU 3 to BU 5) and "10MHZ_RW" 50BU 2 (BU13 [64] on the instrument back panel) if the 400 MHz PLL is locked, as these output signals are derived from the 400 MHz oscillator by division (see section 6.4.3.3, "Timebase 2 (400 MHz PLL)" on page 6-37). The frequency accuracy of the standard frequency oscillator can be measured within the framework of the synthesizer module using e.g. a frequency counter. The stability of the counter directly affects the reliability of the measurement.

6.4.2 YIG oscillator

The general function of the YIG oscillator can be checked as follows:
Connect the YTO RF output BU10 or the synthesizer RF output "1.LO" [71] (on the instrument back panel) to a spectrum analyzer and measure the signal. Open wire link (50)S1 and close switch S3. This interrupts the control loop (S1) and limits the gain of the PI controller (IC26) to a finite value (S3). This setting drives the YTO to the lower limit (2.8 GHz if the lower YTO limit is properly adjusted).

If this lower limit does not result, the YTO can be tuned directly by connecting a DC source between contacts TC+ and TC- of the YTO (disconnect and feed in at H011 and H04). Check the YIG oscillator against the following table; the actual frequency values may differ slightly due to component tolerances in the YIG oscillator.

The YTO frequency is actually governed by the current through the tuning coil.

If the YIG oscillator is not faulty, check the signal path between (50)S1 Pin3 and TP22 (see section 6.4.4.1 on page 6-38).

Frequency	U (H011 - H04)	Frequency	U (H011 - H04)
3.1 GHz	1.9 V	5.5 GHz	3.5 V
3.5 GHz	2.2 V	6 GHz	3.9 V
4 GHz	2.5 V	6.5 GHz	4.2 V
4.5 GHz	2.9 V	7 GHz	4.5 V
5 GHz	3.2 V	7.5 GHz	4.8 V

Table 6-39 YTO frequency as a function of control voltage

Note: If the YIG oscillator is defective, it must be replaced. After replacement of the YIG oscillator, the frequency response of the instrument must be re-determined as the oscillator output level affects the instrument frequency response (see section 7.5.1).

6.4.3 Timebase/YTO driver [2101-B]

6.4.3.1 Power supply

Supply voltages

The supply voltages for the timebase/YTO driver board [2101-B] are fed in directly from the AC PSU (1) via plug (50) ST 13. Check the voltages against the following table.

Test point	Value
IC41.7	+12 V
IC42.7	+6,5 V
IC43.4	-12 V
IC44.4	-6.5 V
L49	+18 V

Table 6-40 supply voltages for board [2101-B]

Central filter (DC-PREFILTER)

The ± 12 V and ± 6.5 V supply voltages are filtered by active OP filters.

Checking the OP filter circuits

An oscillograph of (e.g.) the +12 V filter control voltage at IC41 Pin 6 (same applies for -12 V and ± 6.5 V) shows a DC voltage of ≈ +1 V. This voltage derives from the residual current from electrolytic capacitor C143 through R265. The superimposed AC signal is the interference voltage on the +12 V line. If control is correct, approximately the same potential (ground) should be present at IC41 Pins 2 and 3. The filter function can be tested by feeding in an interference signal via a transformer.
The DC drop across L41 and R266 is typically 0.2 V.

Filter timebase

The controller function of the OP filters can be checked by approximate equality of the potentials at the positive and negative OP inputs:
The DC voltages at IC8 Pins 3 and 2 are +5 V and at IC9 Pins 3 and 2 they are -5 V. Check that the base-emitter voltages of the transistors is ≈ 0.7 V.

The following voltages are "generated" by filtering the timebase.

Test point	Value
L16/C58	+10.5 V
L13/C52	+5 V
L12/C47	-5.2 V
L17/C61	-10.5 V
L49	+18 V

Table 6-41 Voltages "generated" on the timebase filter board

DC CONTROL/Reference voltage generation

The function of the "-5 VYTO" and "+15 VYTO" reference voltage generators can be checked by measuring the OP input and output voltages. IC40 Pins 2 and 3 should have approximately equal potentials of +5 V with ≈ 12 V at the output. IC29.1 Pins 2 and 3 should both be at approximately ground potential. IC29.1 Pin 1 as well as IC29.2 Pins 5 and 6 should be at approximately -5 V.

6.4.3.2 Timebase 1 (10 MHz external synchronization control circuit)

A 10 MHz signal fed into the "Fext10MHz" input (10 MHz input [62] on the instrument back panel) closes the slow PLL (loop bandwidth ≈ 14 Hz) for external synchronization. This can be verified by a HIGH level at IC4 Pin 8 ("external level") or the equality of the potentials at IC4 Pins 6 and 7. When the loop is locked, PI controller IC6 Pins 6 and 5 are at approximately the same level of ≈ +2.7 V and OP output IC6 Pin 7 is driven linearly. In addition, the two 10 MHz signals at IC31 Pins 3 and 11 are synchronous with a small phase shift (≈ 30 degrees); see also section 6.4.1 on page 6-35. The "external level" AND gate (IC7 Pin 2) and the "Phase meter lock signal" (High level at IC7 Pin 8) produce the status signal "EXT_SYNC", St9 Pin 18. The function of the second status signal, "OFEN_WARM" is checked by measuring the voltage drop across R14 and by calculating the current drawn by the heater for the standard frequency oscillator. Comparator IC6.1 should flip to HIGH for currents of ≈ 250 mA.

6.4.3.3 Timebase 2 (400 MHz PLL)

The function of the 400 MHz PLL can be tested by checking that the voltages at PI controller IC35 Pins 3 and 2 are approximately equal (≈ 2.75 V). The control voltage at IC35 Pin 6 should be between 4 and 6 V. The frequency divider chain is checked by tracing the signal path.
A 400 MHz sinusoidal signal at ≈ 7 dBm appears at connector MT65.The 10:1 ECL divider output IC3 Pin 11 yields a 40 MHz FACT level; the first 2:1 divider IC12.1 Pin 5 yields a 20 MHz FACT level, with the 10 MHz FACT level appearing finally at 2:1 divider IC12.2 Pin 9. This latter is fed into the comparator input of phase meter IC32.1 Pin 3. All signals have a duty cycle of 1:1. The timebase reference signals "20MHZ_1" to "20MHZ_3", the 20 MHz ECL pulse to the synchronous divider/phase meter, and the 10 MHz signal "10MHZ_RW" are all divided down from the 400 MHz oscillator and are thus only synchronous with the standard frequency oscillator when the 400 MHz PLL is locked. The PLL can be disconnected at link BR4 for manual tuning of the 400 MHz oscillator (a variable DC source is connected to BR4 Pin 1).

6.4.4 400 MHz oscillator [2101-F]

The frequency of the 400 MHz LC oscillator can be offset by opening solder link BR4 and connecting a variable voltage source to BR4 Pin 1. Connect the RF output socket BU7 "400MHZ" to a frequency counter for measurement. The oscillator should be tunable from about 397 MHz to 403 MHz for an input voltage of ≈ 3 to 9 V, with a slope of ≈ 1 MHz/V in the working range (≈ 4...6 V). The level at RF output BU7 "400MHZ" settles at ≈ 0 dBm/50 Ω.

Typical circuit working points

Test point	Value	Notes
T403 /S	≈ +1.3 V	Source connection S (= -Ugs)
HO63	≈ -4.3 V	
T402 /E	≈ -0.3 V	Emitter, transistor T402
T404 /E	≈ -0.5 V	Emitter, transistor T404
T401 /G1	≈ -0.6 V	Gate 1 G1 of T401
T401 /S	≈ -0.4 V	Source connection S (Ug1s = -0.2 V)
T401 /G2	≈ 3.8 V	Gate 2 G2 of T401 (Ug2s ≈ +4.2 V)

Table 6-42 Typical working points for the 400 MHz oscillator

6.4.4.1 Regulator/YTO driver

The individual components of the regulator/YTO driver can be checked by measureemnt with the control loop disconnected. Open wire link S1 and connect an AC voltage source (+ signal to S1 Pin 3, - signal to S1 Pin 1). If an AC signal with F = 20 kHz and 100 mVpp is fed in and the D.U.T. is set as below, the signal path measurement values in table 6-43 will be obtained.

D.U.T. settings

FSPAN 0 Hz
RUN MAN

Test point	Value
S1 Pin 3	100 mVpp
IC22.7	100 mVpp
IC22.1	100 mVpp
TP2	200 mVpp
TP12	200 mVpp
TP22	150 mVpp

Table 6-43 Test points in the YTO diver signal path

Check the signal path in this setting with a control bandwidth setting of 10 kHz (default). The signal path can be checked at the other control bandwidths in the same way.

Note: Exact settings of the control bandwidth using the analog switch (control signals DS(0) to DS(15)) for switching through a specific path must be made via the DSP of the synthesizer controller. This can only be done in specially equipped service centers as special equipment is required.

YTO frequency limiter

The YTO frequency limiter IC38.1 to IC38.4 must be inactive when the YTO current is within the frequency range (1st LO in the range 3 to 8 GHz), i.e. a negative potential of <0 V must be present at IC38.2 Pin 7 (upper limit control output) as well as at IC38.3 Pin 8 (lower limit control output).

YTO synchronization monitor

In parallel with the controller signal path, the arithmetic mean of the phase meter output at test point TP13 is measured by double-way rectifier IC17.2 and IC17.4, and fed to Schmitt trigger IC17.3. This generates the status signal "YTO_SYNC" indicating synchronicity in CW operation (FSPAN = 0).
The circuit function can be tested by unplugging the contacts BU11 "PD+" and BU12 "PD-" and feeding in a (e.g.) 1 kHz sinusoidal signal into BU12. The arithmetic mean Ua = 2*Up/π (Up is the peak value set at TP13) appears at IC17.4 Pin 14 or IC17.3 Pin 9. The Schmitt trigger should trigger as per its characteristic (on level Uon ≈ 120 mV, off level Uoff ≈ 60 mV).

6.4.5 Synchronous divider/Phase meter [2101-K]

Note: Specific troubleshooting is only possible on this board if the gate array (PLLIA) can be programmed. This requires special equipment and can therefore only be carried out in sppecially equipped service centers.

6.4.6 Synthesizer controller [2101-A]

6.4.6.1 Controller filters

The active OP filters which operate in addition to the central filters are identical in principle to those described in the section "Filter timebase" on page 6-36 (q.v.).

6.4.6.2 Control

The 20 MHz clock for the DSP (digital signal processor) is derived from the timebase (contact HO18 connected to HO17). It can be output to an oscilloscope from IC1 Pin 127 (link HO17-HO18).

Caution!

The DSP can be destroyed if the clock signal is missing.

For AT bus address decoding, first check the synthesizer base address set by BR3 to BR8 and BR11. Links BR8 to BR5 and BR11 must be closed, BR4 and BR3 must be open.

Interrupt and clock generation

To generate the interrupt and clock periods, a 10 MHz signal "CLK_10MHz" is fed to IC 34 Pin 10 as a divider input signal. The following signals are produced: at output "Q2" IC34 Pin 7 2.5 MHz, at "Q4" IC34 Pin 5 625 kHz (1.6 s) and at "Q12" IC34 Pin 1 2.44 kHz (409.6 µs). The long-term interrupt "INTB" IC33 Pin 3 ("Q13") is 3.36 sec (≈ 300 mHz).

Address decoding

Specific troubleshooting of the address decoding requires special control software and equipment and can therefore only be carried out in sppecially equipped service centers.

Checking the interfaces

Specific troubleshooting of the 8-bit output ports IC19, IC30 and the 8-bit input port IC18 requires special control software and equipment and can therefore only be carried out in sppecially equipped service centers.

6.4.7 SHF pre-divider module

The SHF pre-divider module is fed with the YTO signal "FYTO" from socket (50)BU10 in the frequency range 3.1 to 8 GHz. The output signal must be this signal divided by 16.

The SHF pre-divider module can be tested at the lower limit frequency of the YTO. To drive the YTO to the lower limit, proceed as follows:

Open wire link (50)S1 and close switch S3. This interrupts the control loop (S1) and limits the gain of the PI controller (IC26) to a finite value (S3). This setting drives the YTO to the lower limit (2.8 GHz if the lower YTO limit is properly adjusted). Connect the YTO RF output BU10 or the synthesizer RF output "1.LO" [71] (on the instrument back panel) to a spectrum analyzer and measure the signal. Then measure the output signal of the SHF pre-divider module.
The results should be as below:

SHF pre-divider module input
Lower limit: FYTO approx. 2.8 GHz

SHF pre-divider module output
FYTO /16 = 175 MHz (FYTO signal divided by 16)

If the input frequency divided by 16 is not measureable at the output of the SHF pre-divider module, the complete SHF pre-divider module should be replaced. The information in section 2.3 should be observed.

7 Adjustment instructions

7.1 Introduction

After repairing a circuit board or module, follow the relevant adjustment instructions (see section 7.2 on page 7-2). Circumstances will determine whether the entire section or only a part of it need to be followed. In case of doubt, perform all the adjustments given in the section. If circuit boards or modules are replaced, the instructions as listed under "List of adjustments required after replacing circuit boards or modules" (see section 7.3 on page 7-4) should be carried out.

Microwave modules and waveguides must not be repaired. They should be replaced as complete units.

The adjustments listed in section 7.5 can only be performed in specially-equipped Service Centers.

Note: When making adjustments, only those screening can covers necessary for accessing the adjustment controls should be removed. In some cases, the covers must not be removed for adjustments. Covers with holes allowing access to the controls should be used. The instrument should have reached thermal equilibrium and be within the nominal ranges of use for the influence quantities when adjustments are being made.

Adjustments fall into the following categories:

- Check sum correction of hardware status for certain circuit boards (see section 7.4)
- Recording of correction data for the measurement section and synthesizer (see section 7.5)
- Manual adjustments (see section 7.6 ff.)

7.2 List of all adjustment controls

Circuit diagram no.	Adjustment control	Notes	Adjustment instructions in section
1	P1	Overtemperature cutout	7.10.2
2	R54	Reference tuning voltage, 4 GHz VCO	7.6.2
	R20	PLL breakthrough frequency	7.6.2
5	P101	External mixer bias	7.6.1
	P102	External mixer bias	7.6.1
	P103	-	-
6	L1	400 MHz oscillator adjustment	7.6.3
	P1	Frequency converter level adjustment	7.6.3
	R117	Frequency converter level adjustment	7.6.4
7	5 x C86	LC circuit band center frequencies	7.7.1
	5 x P81	LC circuit insertion loss	7.7.1
	5 x C602	Crystal stages stop-band attenuation	7.7.1
	5 x L601	Crystal stages pass-band attenuation	7.7.1
	P7	30 kHz crystal bandwidth	7.7.1
	P8	Bypass path level adjustment	7.7.1
	P4	IF single gain 1 dB	7.7.1
	P2	IF single gain 2 dB	7.7.1
	P6	IF single gain 4 dB	7.7.1
	P5	IF single gain 8 dB	7.7.1
	P1	IF single gain 16 dB	7.7.1
	P3	IF single gain 16 dB	7.7.1
8	P800	+5 V regulator	7.7.2
	P503	Log amplifier working point	7.7.2
	P501	Rectifier threshold voltage (log.)	7.7.2
	P500	Current source bias voltage	7.7.2
	P400	Video amplifier offset	7.7.2
	P401	Adder stage zero point (offset)	7.7.2
	P502	Rectifier threshold voltage (lin.)	7.7.2
	L400, L401, L402	10 MHz video filter	7.7.2
	C227	10 MHz noise filter (symmetry)	7.7.2
	L208	400 kHz noise filter (center frequency)	7.7.2
	10 x P151	10 dB log. amplifier gain	7.7.2

Table 7-1 List of all adjustment controls

Circuit diagram no.	Adjustment control	Notes	Adjustment instructions in section
9	P300	Bipolar offset	7.7.3
	P303	8-bit linearity	7.7.3
	P400	16-bit gain	7.7.3
	P401	16-bit offset	7.7.3
	P301	Overall offset	7.7.3
	P302	Overall gain	7.7.3
	P200	RMS value meter offset	7.7.3
11	P1	External calibration level	7.7.4.1
	P2	Internal calibration level	7.7.4.1
	C317	FM demodulator center frequency	7.7.4.2
	C301	Search demodulator center frequency	-
21	P1	Rotary control offset	7.9.1
50	P101	10 MHz standard frequency	7.8.1
	P2	Upper YTO frequency limit	7.8.2
	P3	Lower YTO frequency limit	7.8.3
	P4	Offset preset (100 Hz control bandwidth)	No adjustment reqd.
	P5	Lower YTO freq. limit (external YTO)	No adjustment reqd.
	P6	Gain, external YTO	No adjustment reqd.
	P7	Gain for internal sinusoidal sweep	No adjustment reqd.
	L406	400 MHz oscillator LC resonator adjustment	7.8.4
51	P1	ADC offset	No adjustment reqd.

Table 7-1 List of all adjustment controls

7.3 List of adjustments required after replacing circuit boards or modules

Note: If an adjustment control is indicated in the column "Adjustment required" the adjustment instructions pertaining to this control in the section indicated must be carried out. If the column indicates a section number only, the entire section including any sub-sections should be followed.

Circuit board or module replaced		Adjustment required	
Circuit board or circuit diagram no.	Name	Adjustment control	Adjustment instructions in section
CG44 (Gossen)	Power supply		7.10.1
2101-BD	Voltage distribution		7.10.2
2101-BE	24/12 V converter		No adjustment
(2), (3), (4),	Any module in the signal path from the input socket to (2) P/J204, including all waveguides. Also YIG filter (3)FI1and input socket	(6) P1, (6) R117	7.6.3, 7.6.4, 7.5.1
2 P38	RF adapter (Rosenberger)		7.5.1
2 AT1	Step attenuator		7.5.1
2 FL1	8 GHz low-pass filter (Suhner)	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2 K1 2101-ZH (2 DX1)	Coaxial relay (series A+ B) Diplexer (from series C on, replaces coaxial relay 2K1)	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2101-ZA	Integration Band 0, complete (series A through E)	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2101-ZA1	Integration Band 0, complete (series E onward)	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2101-ZC	Fundamental mixer, complete	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2101-ZE	IF switch, complete	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
3FL1	YIG filter (ferretec)		7.5.1, 7.5.3
2101-AS1	YIG filter controller		7.5.3
2101-AR	Input section controller		7.6.1
6 IF-1	422 MHz bandpass (Interdigital filter)	(6) P1, (6) R117	7.6.3, 7.6.4
2101-X[1]	422/22 MHz converter	(6) P1, (6) L1	7.6.3
2101-Y* 2101-7023.538 (series A + B)	422/22 MHz/10 kHz converter (for instruments fitted with "narrow bandwidth" option)	(6) R117 (6) C28, C31, C32	7.6.4
2101-Y* 2101-7023.554 (series C on)	422/22 MHz/10 kHz converter (for instruments fitted with "narrow bandwidth" option)	(6) R117 (6) C28, C31, C32	7.6.4

[1] 2101-X or -Y fitted depending on version (2101-Y for narrow bandwidth option)

Table 7-2 List of all adjustments required after replacing circuit boards or modules

Circuit board or module replaced		Adjustment required	
Circuit board or circuit diagram no.	Name	Adjustment control	Adjustment instructions in section
2101-L	IF selection		7.7.1
2101-R	5 x LC bandpass filters (on IF selection)	(7)C86, (7)P81 on circuit board replaced	7.7.1
2101-S	5 x amplifier stages (on IF selection)	Gain potentiometer on board replaced, (7)P1,P3, P5 or P6	7.7.1
2101-M 2101-Q	Logarithmizer 10 x 10 dB log. stages	Gain pot. on board replaced, (8)P151	7.7.2, 7.5.2 7.7.2, 7.5.2
2101-O	IF converter		7.7.3
2101-P	Measurement section controller		No adjustment
2101-N	Calibration generator		7.7.4
2101-AO	Connector board		No adjustment
2101-AG	Interface board (series A to E)		No adjustment, 7.4.5
2101-AF	Memory board		No adjustment, 7.4.6
(18) AT 386	AT CPU (3011-9305.006)		No adjustment, 7.4.7
(18) A1	Floppy disk drive	---	---
2101-AL	Keyboard controller		No adjustment, 7.4.8
2101-AJ	Keyboard		No adjustment
2101-AK	Rotary control		7.9.1
4111-A	Display control board (BSK-3)		No adjustment, 7.4.9
2101-B	Timebase/YTO driver (excluding YTO)		7.8
2101-F	400 MHz oscillator	50L406	7.8.4
2101-C	Standard frequency adapter (NFO adapter)	50P101	7.8.1
50 OS1	YTO YIG oscillator (Sievers)		7.5.1
2101-A	Synthesizer controller	[(51)P1]	Not adjusted in SNA
2101-ZG	SHF pre-divider		No adjustment
2101-K	Synchronous divider / phase meter		No adjustment

[1] 2101-X or -Y fitted depending on version (2101-Y for narrow bandwidth option)

Table 7-2 List of all adjustments required after replacing circuit boards or modules

7.4 Special instructions for replacing circuit boards and modules

Certain measures in addition to the adjustments described are required to ensure correct function when certain circuit boards are replaced. These measures and special instructions are summarized in this section.

7.4.1 Circuit boards with different hardware status

The hardware status for some of the controller boards is stored in an EEPROM on the circuit board. This data is stored when the circuit board is manufactured. This hardware status is read out from the board during the boot-up sequence and is taken into account by the controller during measurement operations. If a circuit board fitted with an EEPROM containing such status data is replaced, the EEPROM contents (check sums) must be checked and corrected if necessary using the "EEPROM" service program. The following circuit boards are fitted with EEPROMs containing hardware status data:

- AT CPU (18)
- Keyboard controller (19)
- Memory (17)
- Interface board (16)
- Display control board BSK-3 (92)

The hardware status of other circuit boards or modules is readable from a port on the board. The status of these boards is set using DIP switches or pull-up/pull-down resistors which are fitted during manufacture. This status is fixed and can be read by the controller for use during measurement operations.

Note: The fixed hardware status of a board must not be changed. If the coded status does not match the actual board status, malfunctions will occur as the board will not be correctly controlled by the controller.

Note: The EEPROM on the interface board (16) alos contains the instrument serial number in addition to the hardware status (see section 7.4.4).

"EEPROM" service program

Starting the service program

Insert the service program floppy disk into drive A: and switch on the instrument. Once the instrument hass booted the operating system from this disk (prompt A:\ appears on the display) type in <EEPROM> using an external keyboard. Once the program has loaded, the display shown on the next page appears:

```
serial number is PR207, id = F88E
CPU EEPROM
3011  7001  0002  0618  1990  0001  0618  1990
0020  0504  1990  0315  0014  0000  0000  0000
55AA  C101  0060  D561  6462  0064  0E65  8066
0067  0068  0069  A06A  C26B  006C  006D  006E
0A6F  55AA  0C08  0000  0000  0000  0000  0000
0000  0000  0000  0000  0000  0000  0000  0000
0000  0000  0000  0000  0000  0000  0000  0000
0000  0000  0000  0000  0000  0000  0000  0C1C
checksum CPU-EEPROM  OK.
checkpat CPU-EEPROM  OK.                          (Press <RETURN> key)
BSK3 EEPROM
4111  7000  0001  0409  1991  5555  AAAA  0000
FFFF  FFFF  FFFF  0972  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  5DA2
checksum BSK3-EEPROM  OK.
checkpat BSK3-EEPROM  OK.                         (Press <RETURN> key)
MEMORY EEPROM
2101  7030  A002  1112  1990  5555  AAAA  0000
FFFF  FFFF  FFFF  0A28  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  5DA2
checksum MEMORY-EEPROM  OK.
checkpat MEMORY-EEPROM  OK.                       (Press <RETURN> key)
CONTROLLER EEPROM
2101  7035  FFFF  FFFF  FFFF  5555  AAAA  0000
FFFF  FFFF  FFFF  0EB9  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  5DA2
checksum CONTROLLER-EEPROM  OK.
checkpat CONTROLLER-EEPROM  OK.                   (Press <RETURN> key)
INTERFACE EEPROM
2101  7031  FFFF  FFFF  FFFF  5555  AAAA  0000
FFFF  FFFF  FFFF  0EB5  FFFF  FFFF  FFFF  FFFF
0004  001E  0005  FFFF  0000  0001  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
F88E  5052  3230  373E  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  5DA2
checksum INTERFACE-EEPROM  OK.
checkpat INTERFACE-EEPROM  OK.
end.
```

Fig. 7-1 "EEPROM" service program display when no check sums were corrected.

If the EEPROM on the interface board does not yet contain the serial number of the instrument, this must first be entered using the program. In such cases, the program branches to a different menu (see section 7.4.5).

Otherwise, the EEPROM content for the AT CPU is displayed first, and the check sums are checked for correctness. Pressing the <RETURN> key causes the next EEPROM to be checked.
If the check sum of one of the EEPROMs is incorrect, the message: <Type "c" to try to correct else any other key> will be displayed. After entering <c>, the incorrect check sum will be recalculated and written to the appropriate EEPROM.

Note: The "EEPROM" service program only corrects the check sums in the EEPROMs. The circuit board hardware status which has been programmed in cannot be altered in this way. Alterations can only be carried out at the factory.

7.4.2 YIG filter control (3) and YIG filter (3) FL 1

7.4.2.1 YIG filter control (3)

Check the settings of the DIP switches before fitting a new board.

There are two Flash EPROMs (U10, U11) on the YIG filter control board; these contain the characteristic curve for the YIG filter (3)FL1.

Three procedures may be followed for replacing the YIG filter control board:

- Replacement of entire board [2101-AS1] including the Flash EPROMs. In this case, the YIG filter characteristic will need to be re-determined and stored (see section 7.5.3).
- Replacement of entire board [2101-AS1] with re-use of the two Flash EPROMs from the old board containing the filter characteristic (unplug EEPROMs froom old board and insert them into sockets on new board). This is of course only feasible if both EEPROMs are undamaged. This procedure avoids re-determining the filter characteristic.
- Replacement of entire board [2101-AS1] including the YIG filter. The filter and filter control are matched, with the filter correction data stored in the EEPROMs of the control board. After replacement, the frequency response of the instrument must be corrected (see section 6.1.1).

Note: After replacement of board [2101-AS1], a thorough check of the function of the YIG filter control for the entire frequency range (bands 1, 2 and 3).

7.4.2.2 YIG filter (3) FL 1

If the YIG filter must be replaced, the characteristic curve must be recorded. See section 7.4.2.1 and section 7.5.3.

7.4.3 Input section controller (5) [2101-AR, 2101-AR1]

DIP switch settings

Before replacing the board [2101-AR], [2101-AR1] check the settings of the DIP switch (5)S2 and correct them if necessary.

Switch	Meaning ON = closed = true
S 2.1	Circuit board 422/22 MHz/10 kHz [2101-Y] fitted (switch = ON when narrow bandwidth option fitted)
S 2.2	Step attenuator control table, bit 0 see step attenuator control table, table 7-4
S 2.3	Step attenuator control table, bit 1 see step attenuator control table, table 7-4
S 2.4	Step attenuator control table, bit 2 see step attenuator control table, table 7-4
S 2.5	Fundamental mixer with preamplifier fitted ? SNA-33 only = ON
S 2.6	Not used
S 2.7	Not used
S 2.8	Not used
S 2.9	Instrument without fundamental mixer (e.g. SNA-20, SNA-30 = ON)
S 2.10	= ON allows bias to be fed in when using an external mixer

Table 7-3 Meanings of switch (5)S2 positions on the input controller board

S2.4	S2.3	S2.2	Step attenuator characteristic (attenuation range/steps/frequency range)
0	0	0	65 dB/5 dB/26.5 GHz (Weinschel 5690-1)
0	0	1	70 dB/10 dB/40. 27 GHz (W&G FED-5/02, HP 33321 G/K)
0	1	0	70 dB/5 dB/4 GHz (W&G FED-5/01)
0	1	1	70 dB/10 dB/4 GHz (Weinschel 151-70)
1	0	0	Not used

Table 7-4 Control table for sellecting various types of step attenuator

Adjusting the coaxial relay operating voltage (series A + B)

The SNA is fitted with various coaxial relays (2) K1 from different manufacturers which operate from different voltages.
Before replacing circuit board [2101-AR] the correct supply voltage (+12 V or +23 V) should be selected for the relay by fitting link R54 **or** R52 (0 Ω resistor).

Note: Coaxial relay 2K1 is replaced by an electronic switch (diplexer) from series C onward. Control of the diplexer (band 0/band 1 to 3) requires fitting of circuit board [2101-AR1], input section control.

Adjusting the step attenuator operating voltage

The SNA is fitted with various step attenuators (2) AT1 from different manufacturers which operate from different voltages.
Before replacing circuit board [2101-AR], [2101-AR1] the correct supply voltage (+12 V or +23 V) should be selected for the step attenuator by fitting link R55 **or** R56 (0 Ω resistor).

7.4.4 Logarithmizer (8) [2101-M]

If the Logarithmizer board (8) [2101-M] is replaced, the correction tables for the new board "pkor_log.tab" and "pkor_lin.tab" must be copied into the instrument. The replacement Logarithmizer module must be completely adjusted (including the files "pkor_log.tab" and "pkor_lin.tab" on floppy disk). The files must be copied to the subdirectories listed below.

- Logarithmizer correction, linear to file: SNA\DATA\ pkor_lin.tab
- Logarithmizer correction, log to file: SNA\DATA\ pkor_log.tab

See also section 7.5.2 on page 7-14.

7.4.5 Interface board (16)

An EEPROM (16 IC18) containing the board hardware status and **the instrument serial number** is located on the interface board. After exchanging the board, the "EEPROM" service program must be started (see section 7.4.1). The following message appears on the display.

```
enter serial number of this device or 'e' = ENTRY OFF to abort
the serial number must be a name with a size of five characters,
beginning with a alpha letter and ending with at least 3 digits!
for example HM002, FM028, PR205 and A0055 are valid serial numbers.
enter serial number of this device

<a0125>                                          (entry of serial number)

serial number = a0125 (y/n)?y                    (confirmation of serial no.)
```

Fig. 7-2 "EEPROM" service program display after replacing the interface board requesting entry of the instrument serial number (input from the keyboard is shown in bold type).

When the correct serial number has been entered, the "EEPROM" service program checks the check sums of all EEPROMs in the instrument and corrects them if necessary (see "Circuit boards with different hardware status" on page 7-6).

Note: If a serial number has already been entered for a new interface board for test purposes, this cannot be changed using the "EEPROM" program. The display shown above only appears when there is no serial number stored in the interface board EEPROM.
The serial number stored in the interface board EEPROM of the instrument is displayed under the menu MODE/CONFIGURATION/HARDWARE/SOFTWARE (see section 3.1.1).

7.4.6 Memory (17)

The entire instrument software including the operating system is stored on the memory board. If this board is replaced because of a fault, the following must be borne in mind:

Check the jumper settings

Jumper P210 must be set to match the memory chip modules used.

P210:
Pin 2,3 ON: 1 Mbit chips
Pin 1,2 ON: 2 Mbit chips. ON = Jumper fitted

P211 sets whether EPROMs or FLASH-EPROMs (U400 through U413 and U500 through U511) are fitted.

P211:
Pin 2,3 ON; Vpp = +5 V ==> EPROMs fitted
Pin 2,1 ON: Vpp = VPROG ==> FLASH EPROMs fitted (default)

Fitting the lithium battery

There is a 512 kB battery-buffered SRAM on the memory board in which the correction tables are permanently stored (see "Recording correction data" on page 7-13). The lithium battery must be fitted before a new memory board is used.

Check and eventual correction of EEPROM check sums

Start the "EEPROM" service program after replacing the memory board (see section 7.4.1). The check sums for the EEPROMs on the memory board are corrected once the program has ended.

Installation of operating system and instrument software

If a new memory board is fitted, the software must be loaded again (see section 4.6).
Once the instrument software has been installed, the SNA should be switched off and then switched on again after a short wait (make sure you remove floppy disks from the drive before switching on again). The isstrument should now boot from the memory board and the normal display should appear on the screen.

Installation of compensation (correction) data

Finally, the compensation data for the SNA must be re-loaded (see section 4.7).

Note: The compensaion data is measured for each instrument individually. A floppy disk which includes this data is supplied with each SNA ("Compensation Data").

7.4.7 AT CPU (18)

After fitting a new CPU, switch on the SNA and make the correct CMOS settings (see section 4.5). Once the setup settings are complete, the instrument re-boots and should exhibit normal boot-up behavior until the measurement screen appears. Switch the instrument off and insert the service disk in the floppy drive <A>. Switch the SNA on to boot it from the service disk and type in <EEPROM> from the external keyboard to start the service program. The check sums contained in all EEPROMs are checked and corrected if necessary.

7.4.8 Keyboard controller (19)

Check all jumpers

Jumpers ST2, ST3 and ST4 must be fitted (shorts).
Links BR1 and BR2 must be closed.

Check and eventual correction of EEPROM check sums

Start the "EEPROM" service program after replacing the keyboard controller (see section 7.4.1). The check sums for the EEPROMs on the keyboard controller are corrected once the program has ended..

7.4.9 Display control board (92)

If this board is replaced because of a fault, the following must be borne in mind:

Check all jumpers

Check that all jumpers are fitted as per "Service manual appendix" (circuit diagram).

Check and eventual correction of EEPROM check sums

Start the "EEPROM" service program after replacing the display control board BSK-3 (see section 7.4.1). The check sums for the EEPROMs on the display control board are corrected once the program has ended.

7.5 Recording correction data

To achieve the high accuracy of the SNA-20/-23, certain modules or components of the instrument must be calibrated. The calibration data is stored in the instrument in the form of correction tables which are applied during measurements made with the SNA.

Note: Correction data can only be recorded by service centers which are specially equipped for this purpose.

Series A through E

The correction data, with the exception of the YIG filter data, are stored on a RAM disk (battery buffered SRAM on board (17), Memory). The RAM disk is drive B:\ and the correction data are located in subdirectory SNA\DATA. The following correction data are determined and stored for each SNA:

Frequency response Band 0 through Band 3

- Frequency response correction, Band 0 File: SNA\DATA\ fckor_b0.tab
- Frequency response correction, Band 1 File: SNA\DATA\ fckor_b1.tab
- Frequency response correction, Band 2 File: SNA\DATA\ fckor_b2.tab
- Frequency response correction, Band 3 File: SNA\DATA\ fckor_b3.tab

Logarithmizer characteristic, linear and logarithmic

- Logarithmizer correction, linear File: SNA\DATA\ pkor_lin.tab
- Logarithmizer correction, logarithmic File: SNA\DATA\ pkor_log.tab

YIG filter characteristic

The YIG filter characteristic is determined individually and stored in Flash ROM on the YIG filter controller.

Series F onwards

The correction data, with the exception of the YIG filter data, are stored on the built-in hard disk.

7.5.1 Frequency response adjustment, bands 0, 1,2 and 3

If any module in the signal path from the input socket [12] through to (6)J1 including all waveguides is repaired or replaced, adjustment of the frequency response is necessary. The synthesizer output level (1st LO) also affects the frequency response of the instrument. If the YTO oscillator of the synthesizer is replaced, frequency response adjustment is necessary.

Frequency response correction values are determined using a special test setup and software. Correction tables are generated and stored in the SNA for each receive band (Band 0, 1, 2 and 3). These correction values are applied mathematically to the results of normal measurements displayed by the SNA.

Recording of frequency response correction values requires complex computer-controlled equipment and can therefore only be performed in service centers specially equipped for this purpose.

7.5.2 Logarithmizer characteristic

This measurement generates and stores the correction table values for the logarithmizer characteristic.
Here, too, a special software-controlled test setup is required for determining the logaritmizer correction values. The software supports recording of the uncorrected logarithmizer characteristic and the calculation of the correction data for both "linear" and "logarithmic" operating modes (see section 7.5 on page 7-13).

Recording the logarithmizer characteristic requires complex computer-controlled equipment and can therefore only be performed in service centers specially equipped for this purpose.

7.5.3 YIG filter (3) characteristic

The YIG filter (band-pass) is tuned by a control current. The relationship between the control current and the filter frequency is non-linear and differs for each YIG filter. For this reason, the characteristic relationship between current and tuning frequency is recorded for each YIG filter. The YIG filter characteristic is determined using a special software-controlled setup and stored in the SNA in Flash EPROMs (U10, U11) on the "YIG filter controller" board (3), [2101-AS1]. If the YIG filter or the "YIG filter controller" board (3), [2101-AS1] is replaced, the YIG filter characteristic must be recorded and stored for the new components (see section 7.4.2 on page 7-8)

Recording the YIG filter characteristic (correction values) requires complex computer-controlled equipment and can therefore only be performed in service centers specially equipped for this purpose.

7.6 Frequency converter adjustments

7.6.1 Input section controller (5) [2101-AR]

Adjusting the external mixer bias current

Switch off the instrument and unplug the ribbon cable from socket P4. Close switch S2.10 (Bias on setting).
Connect contact P4.1 of socket P4 to an ammeter (digital multimeter with range ± 20 mA DC) and switch the instrument on.

5P102 Adjustment: Select the "External mixer" menu and initially enter a value of 12.8 mA for "External mixer bias".
Adjust trimmer P102 (input section control) so that the digital multimeter displays a current value of +12.8 mA ± 0.05 mA.

5P103 In the "External mixer" menu enter a value of 0 mA. Adjust trimmer P103 so that the digital multimeter displays a current value of 0 mA ± 0.05 mA.

7.6.2 "Band 0 frequency conversion control" (2) [2101-CF]

Adjustments required after replacing the " Band 0 frequency conversion control" board (2) [2101-CF]

Note: The Band 0 frequency conversion control board (2) [2101-CF] should only be replaced under exceptional circumstances by experienced and specially-equipped Service Centers, as the adjustment is very difficult. A minimal error in the adjustment can lead to temporary outage of the 4 GHz VCO e.g. when temperature changes occur.
Under normal circumstances, the entire microwave module should be replaced.
The Band 0 frequency converter module (including controller) is available as a spare part. The module is adjusted in the factory, and no further adjustment is necessary.

PLL breakthrough frequency

2R20 The PLL breakthrough frequency is determined by the value of resistor R20. The value of the resistor is determined by a program which takes the slope of the VCO tuning characteristic and the phase detector slope into account. The determination can only be performed in the factory at present.

If the control board is replaced, the value of R20 on the old board should be noted and the same value fitted to the new control board.

Reference tuning voltage

2R54 The reference tuning voltage is adjusted using potentiometer R54. The VCO must first be allowed to run uninterruptedly for 3 minutes, locked to a frequency of 4.000 GHz. If the VCO is not locked by this time, adjust R54 until the VCO locks (U_TP4 typically -6 V to -7 V). Connect a DVM between TP4 and TP6, and adjust R54 to give a value of 50 mV. Make sure that the VCO remains locked during the adjustment.

7.6.3 422 MHz/22 MHz converter (6) [2101-X]

For instruments not fitted with the "Narrow bandwidth" option.

Level adjustment

6P1 Connect a level generator to the measurement input of the device under test and connect a spectrum analyzer to the IF output of the 422 MHz/22 MHz converter 6BU2.

Instrument settings

D.U.T.:	
MODE	SPECTRUM ANALYSIS (CW)
FCENT	22 MHz
FSPAN	0 Hz (RUN MAN)
REFERENCE	0 dBm
ATTN	40 dB
Level generator:	
F	22 MHz
L	0 dBm (50 Ω)
Spectrum analyzer:	
MODE	SPECTRUM ANALYSIS (CW)
FCENT	22 MHz
FSPAN 5 MHz	
REFERENCE	-30 dBm/1 dB/DIV (SCALE 10 dB)

Use the spectrum analyzer to measure the level at IF output 6BU2 and use 6P1 to adjust the level to -30 dBm (50 Ω).

Adjustment of 400 MHz oscillator

6L1 Open the circuit bridges 6 L 1 (printed inductances) until the voltage at 6GL4 is 5.2 V ± 0.2 V.

7.6.4 422 MHz/10 kHz converter (6) [2101-Y]

For instruments fitted with the "Narrow bandwidths" option.

Level adjustment

6R117 Connect a level generator to the measurement input of the device under test and connect a spectrum analyzer to the 21.99 MHz output 6J12.

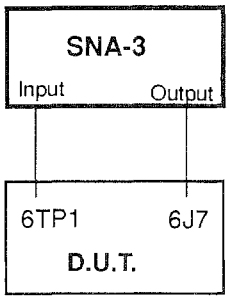
Instrument settings: see level adjustment in section 7.6.3.

Use the spectrum analyzer to measure the level at 6J12 and adjust using 6R117:
Series A, B: to -30 dBm (50 Ω)
Series C on: to -34 dBm (50 Ω)

Adjustment of 21.99 MHz crystal band-pass filter

6C28, C31, C32

Test setup



CAUTION: Remove all other RF cables from 2101-Y, otherwise the cutoff poles will be worse.

Fig. 7-3 Test setup 2 for adjusting calibration level

Initial instrument settings

SNA-3:

NETWORK ANALYSIS	
FCENT	21,99 MHz
FSPAN	10 kHz
REFERENCE	+6.5 dB
RBW	100 Hz
VBW	150 Hz
Sweeptime	1 s
SCALE	0.5 dB/Div.
SEND LEVEL	-12 dBm
GENERATOR	ON

Normalize the SNA-3.
When measuring at TP1 ensure good earth contact and a short inner conductor.

Adjusting the passband

Use C28, C31 and C32 to adjust the passband to < 0.3 dB at 21.99 MHz ± 2 kHz.

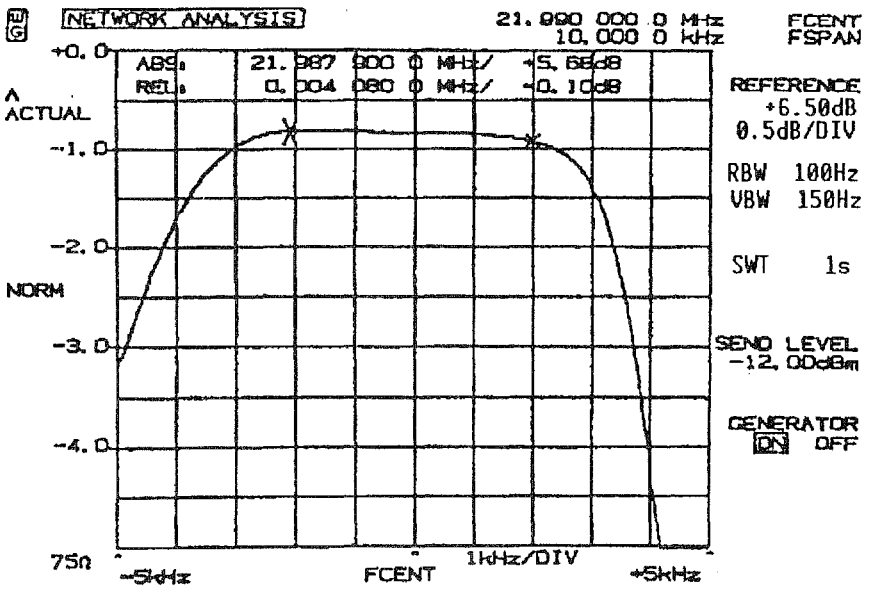


Fig. 7-4 21.99 MHz crystal band-pass filter passband

Adjustment (check) of stop-band

Set the SNA-3 to FCENT = 22.01 MHz.

Adjust cutoff pole using C28 at 22.010 MHz
C31 at 22.008 MHz
C32 at 22.012 MHz

Requirement: at 22.01 MHz ± 2 kHz: < -90 dB

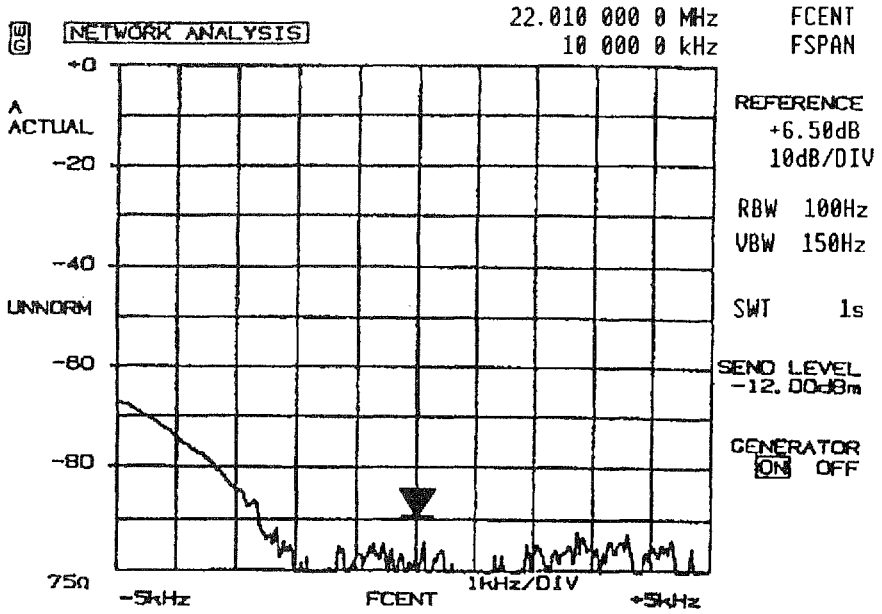


Fig. 7-5 21.99 MHz crystal band-pass filter stop band

Note: The adjustments affect one another. The passband should be rechecked (and readjusted if necessary) after adjusting the stop band.

7.7 IF measurement section adjustments

7.7.1 IF selection (7) [2101-L]

Test equipment and D.U.T. settings

SNA-3:	
SEND LEVEL	-15 dBm/75 Ω
FCENT	21.99 MHz
PSS-16:	
L	-24.3 dBm/75 Ω
D.U.T.:	
Reference	0 dBm

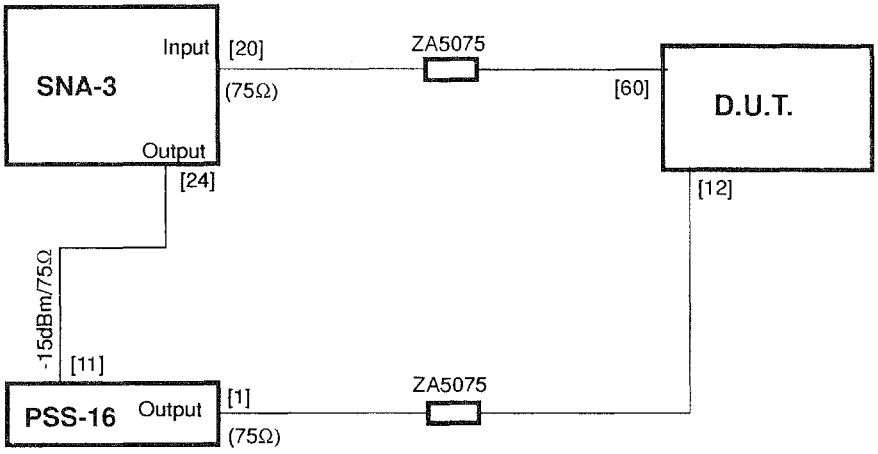


Fig. 7-6 Test setup for adjusting the IF selection

Adjustment of LC circuits

Select the maximum measurement bandwidth in the LC path of the D.U.T. (RBW = 3 MHz). Close links BR15.1-16. This connects the varicap diodes GL82 to an average tuning voltage of +5 V.

Adjustment of band center frequency

7C86 Use S1.6 to set the LC band-pass filter FI1 to minimum bandwidth (approx. 80 kHz). Set the SNA-3 to a SPAN of 1 MHz and adjust C86 (ceramic plate trimmer) on FI1 to give an attenuation minimum at 21.99 MHz (screening can lids with holes for adjustment must be fitted). If the screening can lids are not available, the adjustment can also be made but the attenuation minimum should be adjusted at f = 21.91 MHz.

Adjustment of insertion loss

7P81 Set switch S1.6 to the measurement setting and measure the level using the SNA-3 (SNA settings same as for adjustment of band center frequency). Now close switch S1.6 again (test setting) and adjust potentiometer P81 of FI1 to give a level value which is 0.5 dB higher than that obtained previously with S1.6 open.

Follow the same procedure for adjustment of the other LC stages FI2, FI3, FI4 and FI5, making sure that only the stage to be adjusted is set to the minimum bandwidth with S1.6 through 10.

> ***Caution!***
>
> The temperature of the LC modules [2101-R] FI1, FI2, FI3, FI4 and FI5 must remain constant during adjustment (avoid drafts) as the circuits contain temperature compensation components (C7, R7).
> Fitting the screening covers to the cans shifts the LC circuits by about +80 kHz compared with the adjustment without the covers.
>
> **After completing adjustment, close the links BR15.1 - 15.2again!**

Adjustment of crystal stages

Select a measurement bandwidth for the crystal path of 30 kHz (RBW = 30 kHz).
All crystal stages except the one to be adjusted are bypassed using the links provided for this purpose (see figure 7-7 on page 7-20).

Adjustment of symmetry (stop-band attenuation)

7C602 Set the SNA-3 to a SPAN of 2 MHz to adjust the stop-band. Using the C trimmer C602 of the crystal stage being adjusted, set the stop-band attenuation at the sweep limits to the maximum possible **identical** values. None of the side resonances should be less than the minimum attenuation of 16 dB referred to the pass-band attenuation.

Adjustment of pass-band attenuation

7L601 Set the SNA-3 to a SPAN of 50 kHz to adjust the pass-band attenuation.
Use L601 (shell core) to set the broadest attenuation characteristic with attenuation minimum at f = 21.99 MHz.

Adjust all the crystal stages using this procedure (without screening covers fitted).

Links BR1 through BR14 must be set as follows for the adjustments:

Crystal stage	Links closed
1	BR1.1 - 1.2; 3.1 - 3.2; 5 - 6.1; 7.1 - 8; 9.1 - 10.1; 11.1 - 12.1; 13.2 - 14
2	BR1.1 - 2; 4.1 - 4.2; 6.1 - 6.2; 7.1 - 8; 9.1 - 10.1; 11.1 - 12.1, 13.2-14
3	BR1.1 - 2; 3.1 - 4.1; 5 - 6.1; 7.1 - 7.2; 9.1 - 9.2; 11.1 - 12.1; 13.2 - 14
4	BR1.1 - 2; 3.1 - 4.1; 5 - 6.1; 7.1 - 8; 10.1 - 10.2; 11.1 - 11.2; 13.2 - 14
5	BR1.1 - 2; 3.1 - 4.1; 5 - 6.1; 7.1 - 8; 9.1 - 10.1; 12.1 - 12.2; 13.1 - 13.2

Fig. 7-7 Links which must be closed for adjustment of the IF selection crystal stages

Link and switch settings for normal measurement operation

The links must be set as follows for normal measurement operation:

BR1.1 - 1.2; 3.2 - 4.2; 6.1 - 6.2; 7.1 - 7:2; 9.2 - 10.2; 11.2 - 12.2 und 13.1 - 13.2.

All switches of S1 must be set to "OFF".

Adjustment of 30 kHz crystal bandwidth

7P7 Set all switches S1of the D.U.T. to "OFF", all links to normal measurement operation and set RBW = 30 kHz. Test setup is as for adjustment of the LC filters (see figure 7-6 on page 7-19) .
Set the SNA-3 so that the pass-band of the crystal filter (FCENT = 21.99 MHz) is visible on the screen. Use P7 to adjust the 3 dB bandwidth to B_{max} = 31 kHz.

Adjustment of IF gains

Attenuation matching of the crystal, LC and bypass paths

7P8

Note: Only the attenuation of the bypass path can be adjusted using (7) P8.

Test setup as in figure 7-6 on page 7-19.

> *Note:* The output attenuator of the PSS-16 is used as reference attenuator for this adjustment. To ensure that the required accuracy for the IF amplifier adjustment is achieved, the output attenuator of the PSS-16 should first be calibrated and the actual value taken into account. A precision step attenuator (e.g. Siemens D2053) can be used instead of the PSS-16. The attenuator settings should then be chosen to ensure that the input level to the IF selection is approx. -32 dBm (50 Ω) for the reference measurement.

Select the LC, crystal and bypass paths consecutively by setting the RBW of the D.U.T. appropriately and measure the displayed level using the SNA-3 Set potentiometer P8 so that the attenuation of the bypass path lies between that of the LC and crystal paths.
The filter path is selected by the RBW setting of the D.U.T.:

- bypass path RBW 10 MHz
- LC filter path RBW 3 MHz
- crystal filter path RBW 30 kHz

Adjustment of IF amplifiers

Test setup as in figure 7-8 on page 7-22. Set the D.U.T. as follows:

FSTART	21.99 MHz
FSTOP	21.99 MHz
ATTN	0 dB
EXT. ATTN	0 dB
SCALE	10 dB
RBW	10 MHz
VBW	10 MHz
REFERENCE	-27 dBm

Reference measurement

Remove link BR17.1 - 17.2 (amplifier V1 ==> v = 1).

Set the PSS-16 (level) and the D.U.T. (reference) as specified for the reference measurement in table 7-5 on page 7-22.

Measure the reference level using the SNA-3.

Note: If the PSS-16 is set to a level of -24 dBm, the level after the ZA 5075 (matching pad) at the input to the IF selection (BU1) will be about -30 dBm (50 Ω). This corresponds to the nominal IF selection input level.

Adjustment

7P1, P2, P3, P4, P5, P6

Switch in the IF single gain stages 1, 2, 4, 8 and 16 dB one after the other individually, reducing the PSS-16 output level appropriately, and use P1 through P6 to adjust each stage to the reference level. Settings for adjusting the amplifier stages are shown in table 7-5 on page 7-22. During adjustment of the 2nd 16 dB amplifier stage (V3), the 1st 16 dB amplifier is also switched on as the instrument software does not allow individual control of this amplifier stage (reference shifted).

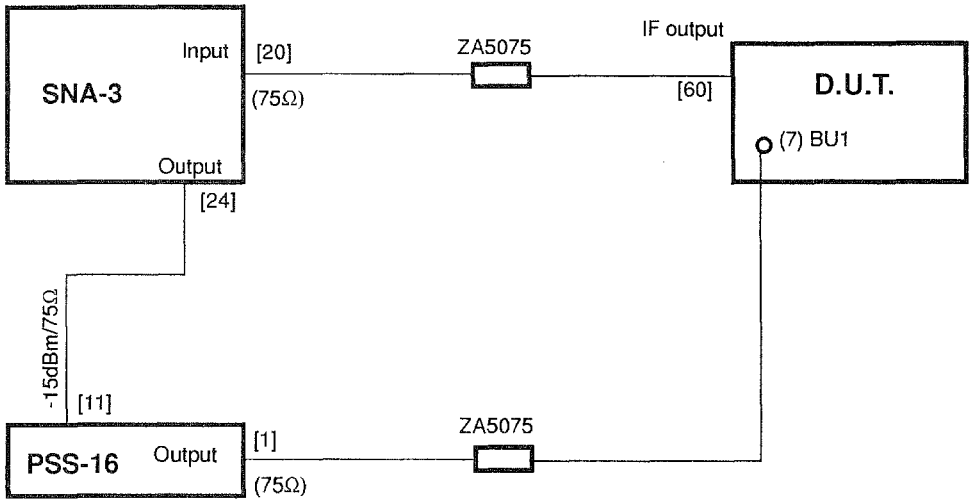


Fig. 7-8 Test setup for adjustment of the IF amplifier stages

Reference D.U.T.	Level PSS-16	V2 0/16 dB	0/-2 dB	V3 0/16 dB	0/-1 dB	V4 0/8 dB	V5 0/4 dB	Adjust using
-27	-26 dBm	0	0	0	0	0	0	Reference measurement
-25	-24 dBm	0	1	0	0	0	0	P2
-26	-25 dBm	0	0	0	1	0	0	P4
-31	-30 dBm	0	0	0	0	0	1	P6
-35	-34 dBm	0	0	0	0	1	0	P5
-43	-42 dBm	1	0	0	0	0	0	P1
-59	-58 dBm	1	0	1	0	0	0	P3

Table 7-5 Parameter settings for adjustment of the IF amplifier stages

Note: "1" in the table means that this stage is switched on. For the 0/-2 dB and 0/-1 dB stages, "1" means that the stage is switched to attenuation (-2 dB, -1 dB).

Frequency response check

Sweep the frequency range 17 MHz to 27 MHz. The attenuation minimum should be at f = 22 MHz.
The increase in attenuation at the limit frequencies must not exceed 2 dB for any IF gain setting.

7.7.2 Logarithmizer (8) [2101-M]

+5 V regulator

8P800 Measure the voltage at TP 21 using a DVM and use P800 to set the voltage to +5.0 V.

The -5 V regulator derives its output from the +5 V and cannot be set independently. During adjustment with P800, make sure that both voltages are within the tolerance of ± 50 mV.

Logarithmic amplifier working point

8P503 Measure the voltage between TP 10 and TP 19 (-12 V U_B) using a DVM and use P503 to set it to +4.0 V ± 10 mV.

Rectifier threshold voltage

8P501 Measure the voltage between TP 8 and TP 9 using a DVM and use P501 to set it to +900 mV ± 1.5 mV.

Current source bias

8P500 Measure the voltage between TP 6 and TP 8 using a DVM and use P500 to set it to - 5.75 V ± 10 mV.

Video amplifier offset adjustment

8P0401, P0400 Set the D.U.T. scale to 100 dB. Open link BR1.1 - 1.2 and close link BR3.1 - 3.2. Measure the voltage at TP24 using a DVM and use P0401 to set it to 1 mV ± 1 mV.
Open link BR3.1 - 3.2 öffnen. Measure the voltage at TP24 using a DVM and use P0400 to set it to 1 mV ± 1 mV.

A high-impedance DVM must be used for this measurement.

****** **Close link BR1.1 - 1.2 again** *****

Adjustment of linear rectifier threshold

8P0502 (Set the SNA to linear scale). Measure the voltage at TP24 using a DVM and use P0502 to set it to 35 mV ± 15 mV.

10 MHz video filter

8L400, L401, L402 Open links BR1.1 - 1.2 and BR3.1 - 3.2 and close link BR2.1 - 2.2 (video test input activated).

Using a spectrum and network analyzer (e.g. SNA-3), determine and adjust the attenuation characteristic of the 10 MHz video filter for "low" (log. scale) and "high" (linear scale) gain. Make the following settings on the spectrum and network analyzer (e.g. SNA-3):

Network Analysis	
FSTART	1 MHz
FSTOP	12 MHz
SCALE	1 dB/DIV
REF	+16 dB
SEND LEVEL	-30 dBm/Z = 75 Ω

Connect the TX output of the SNA-3 to the video test input (8)BU6 of the D.U.T. Connect a high-impedance test probe (TK-11) to the input of the SNA-3 and connect the TK-11 to TP5. Normalize the test setup. Set the D.U.T. to the log. scale 100 dB (= small video gain) and measure at TP24 **(TP24 is DC-coupled!)** using the TK-11. The filter frequency response should

drop off steadily with increasing frequency. The attenuation at the limit frequency of 10 MHz referred to the level maximum at 1 MHz should be 5 dB ± 0.5 dB. Use L400, L401 and L402 to adjust approximately to the trace and attenuation value shown in figure 7-9 on page 7-24.

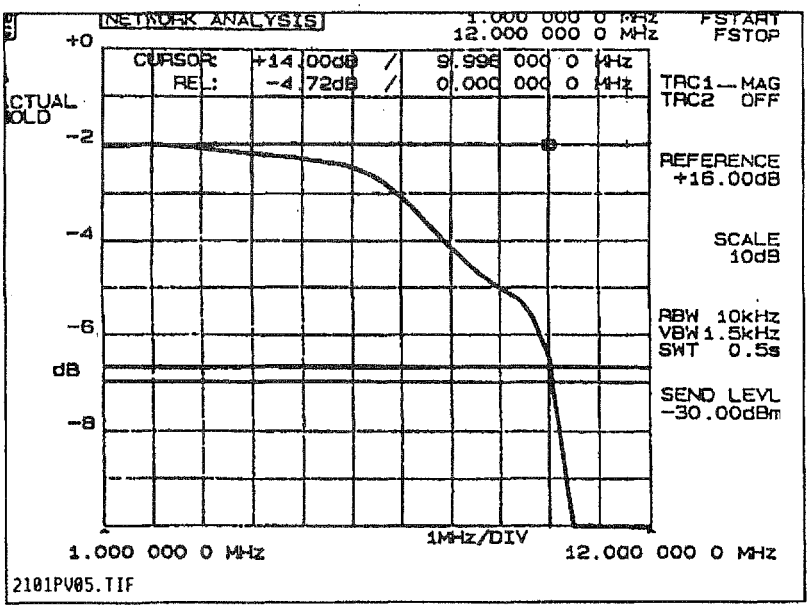


Fig. 7-9 Typical attenuation characteristic of the 10 MHz video amplifier at low gain

Now set the D.U.T. to linear scale (high video gain) and set the REFERENCE on the SNA-3 to +37 dB. The attenuation at the limit frequency of 10 MHz referred to the level maximum at 1 MHz should be 5 dB ± 0.5 dB. Use L400, L401 and L402 to adjust approximately to the trace and attenuation value shown in figure 7-10 on page 7-24.

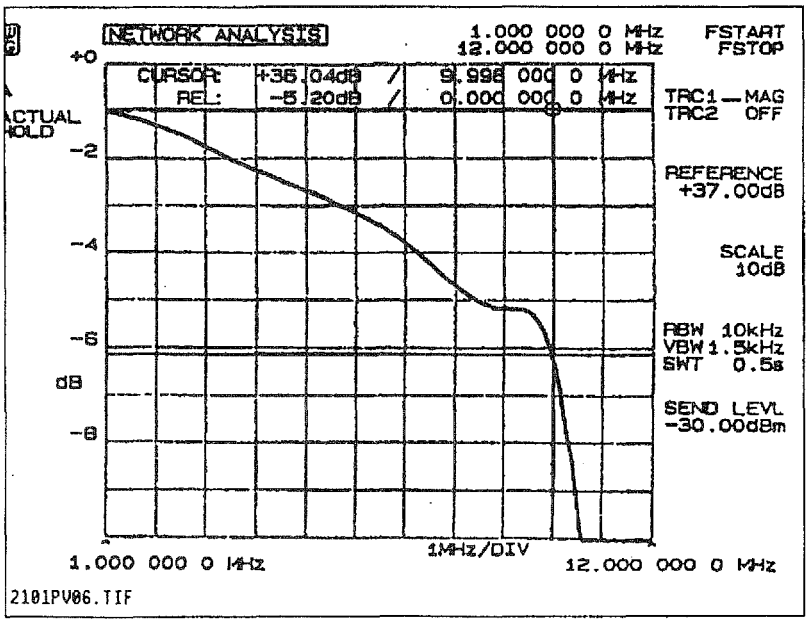


Fig. 7-10 Typical attenuation characteristic of the 10 MHz video amplifier at high gain

As the same adjustment components are used for both adjustments, a trade-off must be achieved such that both measurements lie within the given tolerances.

After completing the adjustment, set all links back to normal measurement positions.

10 MHz noise filter

8C227 Use a spectrum and network analyzer (e.g. SNA-3) to determine and adjust the symmetry of the 10 MHz noise filter (NBW). make the following settings on the spectrum and network analyzer (e.g. SNA-3):

Network Analysis	
FCENT	21.99 MHz
FSPAN	20 MHz
SCALE	0.5 dB/DIV
REF	+1 dB
SEND LEVEL	- 30 dBm/Z = 75 Ω
RBW	30 kHz
D.U.T. settings	
RBW	≥ 1 MHz

Replace log. stage no. 5 with **test board 34-2101** and connect the output of the SNA-3 to the test board socket (noise filter input). Use the TK-11 to measure at one of the two amplifier outputs of log. stage 6 (pin 13 or pin 21) and normalize the SNA-3. Now connect the TK-11 to TP26 or TP27 (noise filter outputs) and adjust the filter using C227 so that the attenuations at 21.99 MHz are symmetrical and 0.5 dB below the normalization trace (see figure 7-11 on page 7-25). The permitted deviation from the reference value (normalization trace) for FCENT ± 4 MHz is +0.2 dB to -1.2 dB.

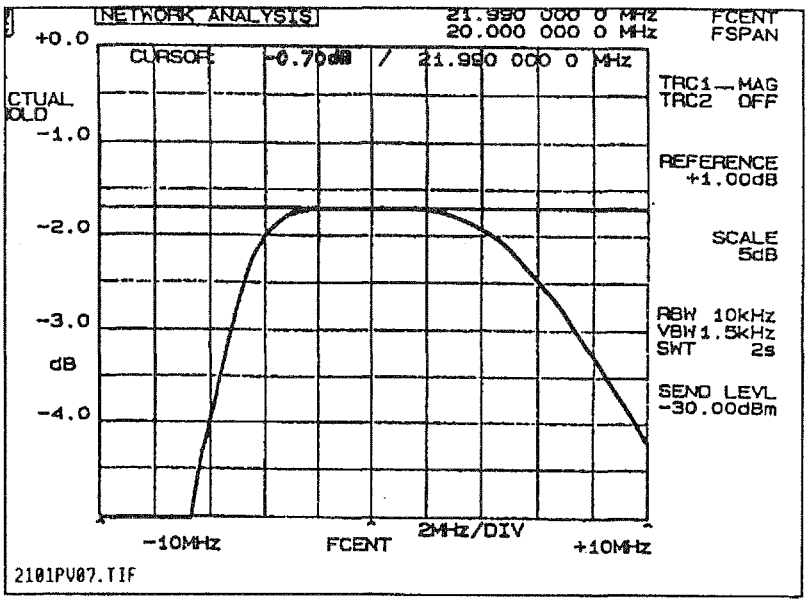


Fig. 7-11 Typical attenuation characteristic for the 10 MHz noise filter (bypass path)

Adjustment of the 400 kHz noise filter

8L208 The center frequency and gain of the 400 kHz noise filter are set automatically by computer-controlled calibration equipment. The center frequency is set with a control voltage between 0 and -11 V at (8)TP1; the gain is set with a control voltage between 0 and -11 V at (8)TP2. Adjustment of the center frequency is very difficult without the special test program.

Adjustment without test program

Note: This adjustment should only performed in exceptional circumstances, as p.c.b. tracks must be broken to perform it.

The center frequency calibration and the gain of the noise filter must be disabled for the adjustment (break the p.c.b track between IC82.2 Pin7 and TP1, and between IC64.15 and TP2). Feed a voltage of -3.9 V in at TP1, and feed an average voltage of about -4.5 V in at TP2. Set the noise bandwidth of the D.U.T. to 400 kHz (set the RBW from 1 kHz to 100 kHz, see table 7-6). The test setup and other settings are as for measurement of the 10 MHz noise bandwidth. Set the filter attenuation of the 400 kHz noise filter to 0 dB (normalization trace) by varying the voltage at TP2. Use L208 to set the center frequency of the 400 kHz filter to exactly 21.99 MHz (use L208 and the control voltage at TP2 alternately to achieve a gain of 0 dB at the center frequency). The attenuation characteristics of the noise filter are shown together in figure 7-12 on page 7-26.

Noise bandwidth	Use at resolution bandwidth (RBW)
> 10 MHz (bypass path)	≥ 1 MHz
1 MHz	300 kHz
400 kHz	1 kHz to 100 kHz

Table 7-6 Noise filter settings as dependent on the selected RBW

The peak of the 400 kHz filter trace must lie exactly on the normalization or 10 MHz filter trace at 21.99 MHz.

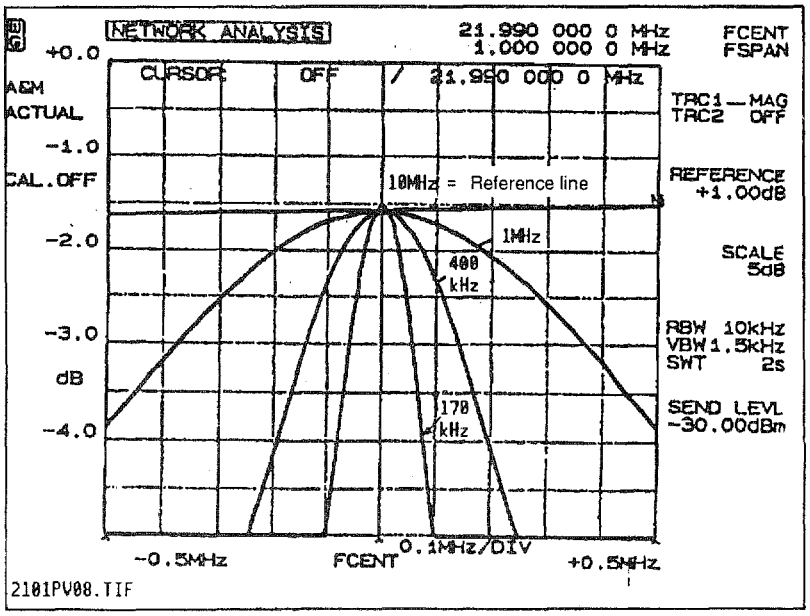


Fig. 7-12 Simultaneous display of all noise filter characteristics

Adjustment of 10 dB logarithmic amplifier gain

8P151 The gain of the 10 dB logarithmic amplifier must be adjusted to exactly 10 dB.

Note: Gain adjustment of the 10 dB logarithmic amplifier requires special test equipment and can only be performed by Service Centers specially equipped for the purpose.

Correction of logarithmizer characteristic

Note: This measurement generates and stores correction tables for the logarithmizer. This requires special test equipment and can only be performed by Service Centers specially equipped for the purpose.

Replacement of p.c.b.

If the "Logarithmizer" board (8) [2101-M] is replaced, the correction values for the new board in the files "pkor_log.tab" and "pkor_lin.tab" must be copied into the instrument. The replacement logarithmizer module must be previously calibrated (including the files "pkor_log.tab" and "pkor_lin.tab" on floppy disk). IThe following files must be copied into the specified directories.

- Logarithmizer correction, linear to file: SNA\DATA\ pkor_lin.tab
- Logarithmizer correction, logarithmic to file: SNA\DATA\ pkor_log.tab

7.7.3 IF converter (9) [2101-O]

Note: Adjustment of the IF converter board requires special test equipment and can only be performed by Service Centers specially equipped for the purpose.

The following adjustments must have been made to the board:

P303, P400 ; P401 • Linearity and synchronism
P301, P302 • Overall gain and offset
P200 • DC adjustment of rms rectifier
P300 • Adjustment of bipolar offset

Replacement of the circuit board

The IF converter module 2101-O is available as a completely adjusted spare part.

7.7.4 Calibration generator (11)[2101-N]

7.7.4.1 Adjusting internal and external calibration levels

Test setup 1

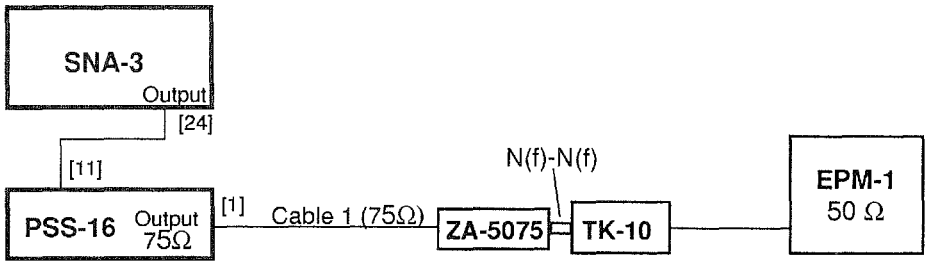


Fig. 7-13 Test setup 1 for adjustment of calibration level

Test setup 2

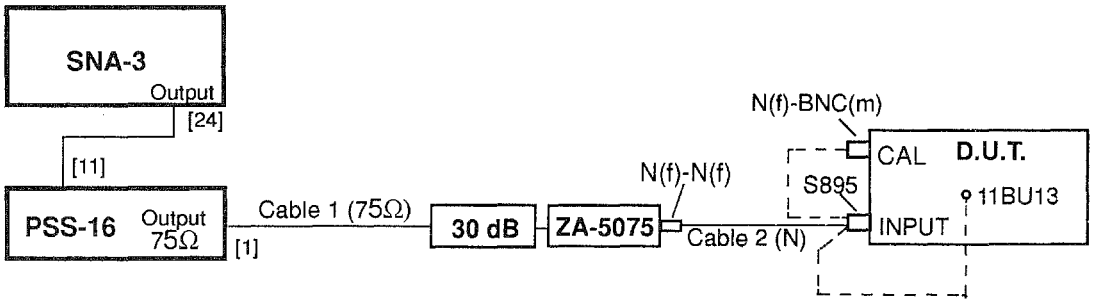


Fig. 7-14 Test setup 2 for adjustment of calibration level

Initial instrument settings

SNA-3:	NETWORK ANALYSIS	
	FCENT	21.99 MHz
	FSPAN	0 Hz
	SEND LEVEL	-15 dBm
	GENERATOR	ON
PSS-16:	Level	+5.8 dBm
EPM-1, 50 Ω:	0 dBm, R_i = 50 Ω	
D.U.T.:	PRESET, SPECTRUM ANALYSIS (CW)	

Enabling permanent operation of the CAL output:

- Connect a PCkeyboard to the D.U.T. socket [1].
- Press Alt + F10 followed by ENTER (sets instrument to DOS mode)
- If necesary, match the keyboard driver (see section 4.10).
- Further entries: set calout=1 ENTER
  k ENTER (returns to measurement program)

--> Permanent operation is now enabled but not activated.

Further D.U.T. settings:

FCENT:	21.99 MHz
FSPAN:	0 Hz
REFERENCE:	-29.5 dBm
SCALE:	10 dB
RBW:	1 kHz
VBW:	10 Hz
SWT:	25 ms
ATTN:	10 dB

Providing the reference signal

Calibrate the EPM-1.
Test setup 1 as in figure 7-13.
Adjust the output level of the generator until the EPM-1 indicates a value as near as possible to 0.00 dBm. Note the difference as correction value "X_1".

Measuring the reference signal

Test setup 2 as in figure 7-14 with connection from ZA-5075 to the INPUT of the D.U.T. Make sure that the same ZA-5075 is used as for test setup 1.
Activate the ABS and REL markers (press the "MKR" twice).
The display shows the reference as a trace at approx. -30 dBm.
Use the MARKER / MARKER UPDATE softkeys to set the ABS marker to HOLD. Press RTN to return to the main menu.
This stores the reference signal.

Adjusting the internal calibration level

11P2 Connect the internal CAL output of the D.U.T. (11) BU13 to the input of the D.U.T.
The output signal from the CAL output is displayed with a relative value of approx. -30 dBm.
Note the relative value as "X_2".
-> Nominal value = X_2 - X_1
Use (11)P2 to adjust the relative value to the nominal value.

Adjusting the external calibration level

11P1 Connect the CAL output [11] of the D.U.T to the INPUT using cable 2 (N). Make sure you use the same cable as was used for the reference measurement.
Switch the CAL output on permanently from the CAL menu: Press "CAL.OUTPUT ACTIVE", then "RTN".
The output signal from the CAL output is displayed with a relative value of approx. -30 dBm.
Note the relative value as "X_3".
-> Nominal value = X_3 - X_1
Use (11) P1 to adjust the relative value to the nominal value.

Note: Always adjust the internal calibration level first, as the external level is dependent on both 11P1 and 11P2.

7.7.4.2 FM demodulator center frequency

D.U.T. setting

FCENT 22 MHz

Feed a level of -30 dBm (50Ω) at F = 22 MHz into (7)BU1.

11C317 Measure the voltage between pins (11)IC31.6 and (11)IC31.12 (TP12) using a DVM and use C317 to adjust such that the magnitude of the voltage is <0.3 V.
After this perform the checks as detailed in "Checking the FM demodulator" on page 6-29.

7.8 Synthesizer adjustments

7.8.1 10 MHz standard frequency adjustment

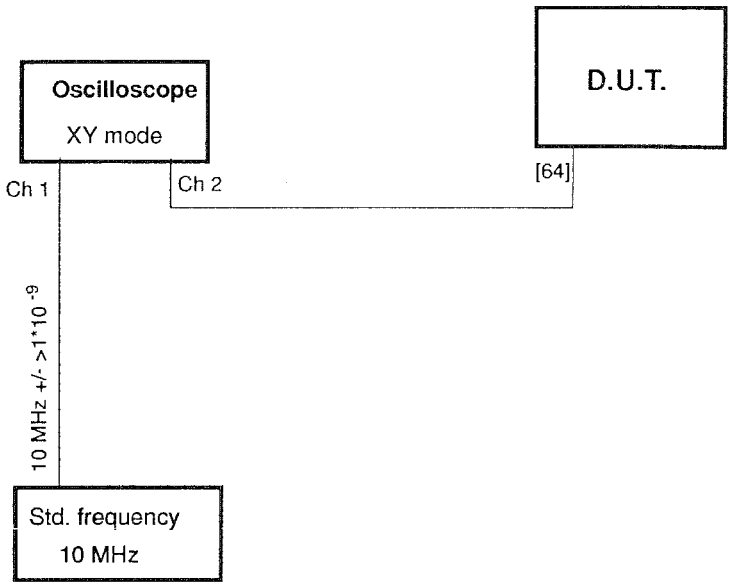


Fig. 7-15 Test setup for adjustment of 10 MHz standard frequency

50P101 Preparation: Allow the instrument to warm up for about 1 hour.

Test setup as per figure 7-15. Set the oscilloscope to X/Y mode. Adjust the instrument's 10 MHz standard frequency using P101 until the Lissajous figure on the oscilloscope screen is practically stationary (a maximum of one rotation in 11 seconds is permitted).

If an external frequency standard is not available, the 10 MHz standard frequency can be measured with a very accurate frequency counter and P101 adjusted to give 10 MHz 0.1 Hz.

Note: The accuracy of the frequency standard or frequency counter used directly affects the frequency accuracy of the SNA.

7.8.2 Upper YTO frequency limit (maximum frequency)

Setting or checking

50 P2

Connect the synthesizer RF output "1.LO" ([71] on the back panel) to a spectrum analyzer. Turn potentiometer (50) P2 to the right as far as it will go. Set D.U.T. FCENT to 7.499 999 999 GHz (FSPAN = 0 Hz, RUN = MAN). The 1st LO frequency must be 7,921 989 999 GHz which should be measurable with the spectrum analyzer connected to socket [71]. Now turn potentiometer P2 to the left until the frequency of the 1st LO just begins to drop. Now turn potentiometer P2 back approximately 1 turn to the right. This sets the upper YTO limit to approx. 8.2 GHz.

Note: Exact setting of the upper YTO limit to 8.2 GHz requires special test equipment and can only be performed by Service Centers specially equipped for the purpose.

7.8.3 Lower YTO frequency limit (minimum frequency)

Setting or checking

50P3

Connect the synthesizer RF output "1.LO" ([71] on the back panel) to a spectrum analyzer. Open switch (50)S1 (wire link) and close switch (50)S3. This interrupts the regulator loop (S1) and limits the DC gain of the PI regulator (50 IC26) to a finite value (S3). This drives the YTO to the lower limit (2.8 GHz when the lower YTO limit is adjusted correctly).
Adjust potentiometer P3 to set the lower YTO limit to 2.8 GHz ± 10 MHz.

7.8.4 400 MHz oscillator adjustment (400 MHZ_RESONATOR)

Note: Adjustment is only required if board 2101-F is replaced.

50L406

Function: LC resonator adjustment in the 400 MHz oscillator (adjustment of printed inductance L406).

Preparation: Adjustment of the 10 MHz standard frequency must have been performed first.

Connect the 400 MHz output "400MHZ" BU7 to a frequency counter. The frequency display should settle as described under adjustment of the 10 MHz standard frequency (if not, adjust the 10 MHz standard frequency). The cover of the 400 MHz oscillator must be closed. Use a DVM to measure the control voltage at IC35 Pin 6. It should be between 4 and 6 V. If not, remove as many links in the printed inductance L406 until the voltage is within this range. The voltage changes by ≈ +2 V for each link removed.

7.9 Controller adjustments

7.9.1 Rotary control (21) [2101 AK]

Adjustment of IC9 offset

21P1 The pulse generator must be idle (do not move rotary control). Use a DVM to measure the voltage between TP1 and ground. Use P1 to set +2.5 V at TP1.

7.10 Power supply unit adjustments

7.10.1 PSU CG44 (1) [Gossen]

Preparation

The PSU is fitted in the instrument and all modules are connected (nominal load).
The following output voltages can be set and should be adjusted. The potentiometers on the PSU are labelled accordingly.

+5 V output voltage

The +5 V rail is measured on the memory board / AT-CPU at plug J2 betwen Pin C29 (+5V) and Pin C31 (ground) and adjusted to **+4.9 to 5.0 V**.
As a check, measure the voltage between the screw connectors MT1/ MT3 (+5V) and MT2 (ground). The voltage must not exceed +5.30 V.

> ***Caution!***
> This adjustment is important for correct function of the instrument. If the +5 V rail is set too low, the instrument may not work at all (does not boot, operates erratically). If the voltage directly on the PSU (MT1/ MT3) is more than +5.30 V the PSU may switch off under certain conditions (overvoltage protection).

+6.5 V output voltage

The +6.5 V rail is measured on the voltage distribution board (1), [2101-BD] at capacitor C16 and adjusted to **+6.8 V ± 0.1 V**.

-6.5 V output voltage

The -6.5 V rail is measured on the voltage distribution board (1), [2101-BD] at connector B8 and adjusted to **-6.5 V ± 0.1 V**.

If the PSU together with the voltage distribution board [2101-BD] is replaced, the adjustments in section 7.10.2 should also be made.

7.10.2 Voltage distribution (1) [2101-BD]

Adjustment of overtemperature cutoff

1P01 Adjustment with P01 should be made when the temperature is measured. The casing cover of the SNA should be placed loose on the instrument (self-heating).
The instrument should switch to "standby" mode at a temperature of > 55 °C (thermal cabinet).
If a thermal cabinet is not available for making the adjustment, set the voltage at IC 5.3 Pin 9 at room temperature to ≈ 4.3 V.

8 Checking the Specifications

8.1 Introduction

This chapter describes methods for checking important specifications and functions. Specifications and functions which can be checked by the user without special instructions or which are automatically checked by test routines built-in to the instrument are excluded.

Unless stated otherwise, the tests should be carried out in a temperate laboratory climate at an ambient temperature of 23 °C ± 3 °C after allowing the instrument to warm up for the specified period.

The checking of the specification serves to establish whether the indicated or displayed measurement value is within the specified error limits. This can only be established without reservation if the error in the measuring equipment used is negligible. The error in the measuring equipment used is added to the error of the device under test when assessing conformance to the specified error limits (IEC Publication 359).

This can be illustrated using symmetrical error limits as an example:

If the error in the measuring equipment used is ± (m) and the specified error limits for the device under test are ± (e), then:

- if the limit ± (e + m) is exceeded, the specified error limits have certainly been exceeded;
- if the limit ± (e - m) is not exceeded, the specified error limits have certainly not been exceeded.

Adjustment of the device under test should only be made if the specified error limits (e) have definitely been exceeded when the measurement error (m) is taken into account.

Safety test

First check the protective ground connector and the insulation resistance. See chapter 2.1.1.

8.2 Measuring Equipment

Recommended measuring equipment for standard checks

Instrument	Requirements	Recommended type	Manufacturer
Frequency counter	Accuracy at 10 MHz: < 0.03 Hz	Any	Any
Synthesizer	10 MHz to (3.2) 26.5 GHz	SNA-(20)/23 + TG-(20)/23 or 83640	W&G HP
Milliwatt power meter	Frequency range DC to 300 MHz with 50 Ω N adapter	EPM-1 (BN 564/01) with TK-10 probe (BN 572/01)	W&G
Level generator	Z_0 = 50 Ω and 75 Ω 1 to 22 MHz; +9 dBm	PSM-39 or PS-19 with ZA-5075	W&G
Power meter with Power Sensor 1	10 MHz to 26.5 GHz 0 to -30 dBm; PC 3.5	438A 8485A	HP HP
Precision attenuator pads	5, 10, 20, 30, 40 dB 3 to 30 MHz N connectors Z_0 = 75 Ω	DG-1405 DG-1410 DG-1420 DG-1430 DG-1440	W&G
Attenuator pad	10 dB; 50 Ω; to 22 GHz; PC 3.5	8493C; Option 010	HP
Terminating resistor	50 Ω; 0 to 26.5 GHz PC 3.5 (f)	909D; Option 011	HP
Z_0 matching pad	N 75 Ω (f) to N 50 Ω (m)	ZA-5075, BN 925/03	W&G
Adapter	EPC to N(f)	S 895	W&G
Adapter	EPC to PC 3.5 (m)	S 896	W&G
Adapter	PC 3.5 (f) to PC 3.5 (f)	S 864	W&G
Adapter	N(f) to N(f), 50 Ω	53 K 101-K00 A3	Rosenberger
Adapter	N(m) to BNC(f), 50 Ω	S 846	W&G
Adapter	N(f) to BNC(m), 50 Ω	51 S 153-K00	Rosenberger
Adapter	N(m) to BNC(f), 75 Ω	73 S 171-K00	Rosenberger
Cable, 61 cm	PC 3.5to PC 3.5 (m - m)	11500E	HP
Cables	N 50 Ω; BNC 75 Ω	K xxx	W&G
1 Power Meter and Power Sensors must be calibrated together.			

Further measuring equipment required for the additional tests in chapter 8.10

Instrument	Requirements	Recommended type	Manufacturer
Network analyzer	Scalar	8757E	HP
2nd synthesizer	10 MHz to 26.5 GHz	83640	HP
Return loss bridge	with calibrated standards	85027B	HP
Directional coupler	1.7 GHz to 26.5 GHz	Type no. 4227-16	NARDA
Power splitter	50 Ω; N connectors 18 GHz	Type 1870A	Weinschel
Low-pass filter	f_{lim}: 900 MHz; a = 60 dB/octave	Type 2001.17F 987-6500.340	Suhner W&G
Low-pass filter	f_{lim}: 1400 MHz; a = 60 dB/octave	Type 2001.17G 987-6500.353	Suhner W&G
Low-pass filter	f_{lim}: 2100 MHz; a = 60 dB/octave	Type 2002.17B 987-6500.337	Suhner W&G
Low-pass filter	f_{lim}: 14 MHz; a = 60 dB/octave	0987-6500.324	W&G
2 Attenuator pads	10 dB / 50 Ω (m/f)	Type 44; 0 to 18 GHz	Weinschel
Attenuator pad	6 dB; SMA	4138060000 0000-7668.351	Radiall W&G
2 Isolators	20 dB isolation; 4 to 8 GHz	Type no. 4914	NARDA
2 Isolators	16 dB isolation; 8 to 18 GHz	Type no. 4946	NARDA

Adapters

The adapters required between the various connector systems (BNC, N, PC3.5, EPC) are not specially indicated in the following test setups (diagrams and text). Various combinations can often be used. If certain adapter types are stated, these adapters should be used.

8.3 Frequency Accuracy

Method 1

Test setup

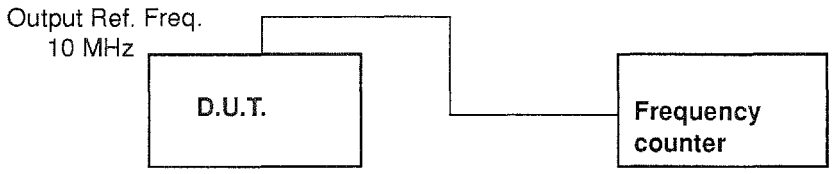


Fig. 8-1 Test setup 1 for frequency accuracy

Equipment required

1 frequency counter (accuracy at 10 MHz: < ± 0.03 Hz)

Measurement

Measure the 10 MHz output. Specified error limit (e) after adjustment: 10 MHz ± 0.1 Hz
Specified error limit (e) after 1 year: 10 MHz ± 0.6 Hz

Method 2

Equipment required

1 Oscilloscope, 2-channel, $f_{lim} \geq 10$ MHz
1 Frequency standard f = 10 MHz ± 0.01 Hz

Test setup

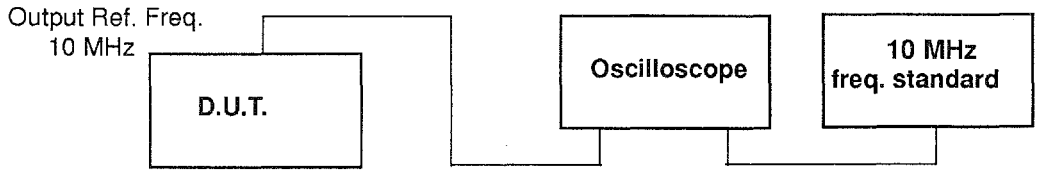


Fig. 8-2 Test setup 2 for frequency accuracy

Connect the 10 MHz standard frequency output of the D.U.T. to channel A of the oscilloscope. Connect the 10 MHz frequency standard to channel B of the oscilloscope.

Instrument settings

Oscilloscope: XY mode

Measurement

Select the sensitivity of channel A and channel B of the ocilloscope such that the display is as close to a circle as possible. The apparent rotation of the displayed Lissajous figure should not be more than one revolution in 10 s after adjustment or one revolution in 2 s after one year.

8.4 External CAL Output Level Accuracy

Equipment required

1 Milliwatt power meter (50 Ω)	EPM-1; 564/01	W&G
with probe (50 Ω)	TK-10; 572/01	W&G
1 Level generator	PSM-39	W&G
1 30 dB attenuator pad	DG-1430	W&G
1 Z_0 matching pad	ZA5075;925/03	W&G

Test setup 1

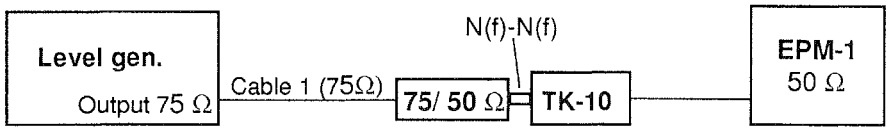


Fig. 8-3 Test setup 1 for external CAL output level accuracy

Test setup 2

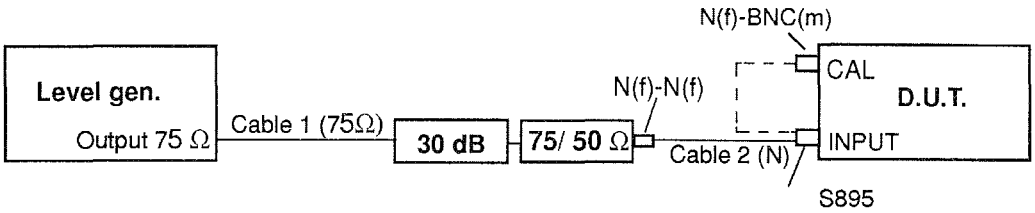


Fig. 8-4 Test setup 2 for external CAL output level accuracy

Initial instrument settings

EPM-1, 50 Ω: 0 dBm, R_{in} = 50 Ω

Level generator:21.99 MHz, +5.8 dBm, R_{out} = 75 Ω

D.U.T.: PRESET, SPECTRUM ANALYSIS (CW)

Set permanent operation of CAL output:

- Connect an external PC keyboard to the D.U.T. [1].
- Press Alt + F10, then press ENTER (switch to DOS mode)
- If necessary, change the keyboard driver (see chapter 4.10).
- Further entries: set calout = 1 ENTER
  k ENTER (returns to measurement program)

--> Permanent operation is now available but not activated.

Further D.U.T. settings:

FCENT:	21.99 MHz
FSPAN:	0 Hz
REFERENCE:	-29.5 dBm
SCALE:	10 dB
RBW:	1 kHz
VBW:	10 Hz
SWT:	25 ms
ATTN:	10 dB

Measurement

Provide a reference signal:

Calibrate the EPM-1.
Test setup 1 as in figure 8-3.
Adjust the output level of the level generator so that the EPM-1 displays a value as near as possible to 0.00 dBm. Note the difference between the displayed value and 0.00 dBm as "X_1".

Measure the reference signal:

Test setup 2 as in figure 8-4, with connection from ZA-5075 to the INPUT of the D.U.T. The same ZA-5075 must be used as was used in test setup 1 !
Activate the ABS and REL markers (Press "MKR" key twice).
The screen displays the reference signal as a line at about -30 dBm.
Use the MARKER / MARKER UPDATE softkeys to set the ABS marker to HOLD. Press "RTN" to return to the main menu.
The reference signal is now stored.

Measure the calibration source:

Connect the CAL output [11] of the D.U.T to the INPUT using cable 2 (N). The same cable must be used as was used for the reference measurement!
Activate the CAL output permanently from the CAL menu: Press "CAL.OUTPUT ACTIVE" then "RTN".
The screen display shows the CAL output signal as a relative value at about -30 dBm.
Note the relative value as "X_2".

-> Nominal value = $X_2 - X_1$

Specified error limit (e): $\leq \pm 0.10$ dB

8.5 Scaling Error

Equipment required

1 level generator 10 MHz	PSM-39	W&G
1 5 dB attenuator pad:	DG-1405	W&G
1 10 dB attenuator pad:	DG-1410	W&G
1 20 dB attenuator pad:	DG-1420	W&G
1 30 dB attenuator pad:	DG-1430	W&G
1 40 dB attenuator pad:	DG-1440	W&G
1 Z_0 matching pad 50 Ω/75 Ω	ZA 5075, BN925/03	W&G

Test setup

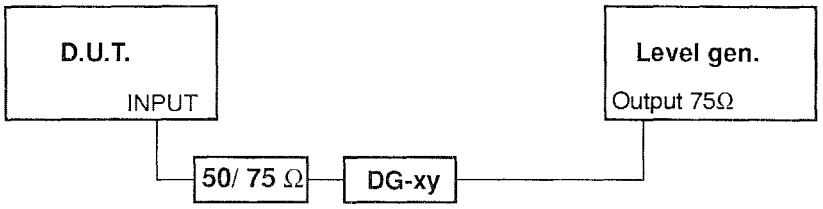


Fig. 8-5 Test setup for scaling error

Instrument settings

Level generator: Z_0: 75 Ω
Frequency: 10 MHz
Level: +9 dBm

D.U.T.: PRESET, SPECTRUM ANALYSIS (CW)
FCENT: 10 MHz
FSPAN: 0 Hz
REFERENCE: 5 dBm
SCALE: 100 dB
RBW: 1 kHz
VBW: 10 Hz
SWT: 100 ms
ATTN: 30 dB

DG-xy: 0 ... 60 dB (as specified below)

Measurement

Reference measurement:
Make a measurement without an attenuator pad (DG-xy = 0 dB).
Measured value: approx. 2 dBm.
Use the MARKER TRANSF / ABS-->REF softkeys to set the line to the reference line.
Activate the ABS and REL markers (press "MKR" twice).
Use the MARKER / MARKER UPDATE softkeys to set the ABS marker to HOLD. Press "RTN" to return to the main menu.
The reference signal is now stored.

Scaling:
Insert the attenuator pads corresponding to the X values in the table and compare the REL level displayed by the D.U.T. with the specified error limits. Up to two attenuator pads may be connected in series.

X / dB	5	10	15	20	30	40	50	60
Error limits* (e) / dB	0.2	0.4	0.5	0.5	0.5	0.5	0.5	0.5

*Valid for T_{amb} = 20 to 26 °C

8.6 Attenuator Error

Equipment required

1 level generator	PSM-39	W&G

Test setup

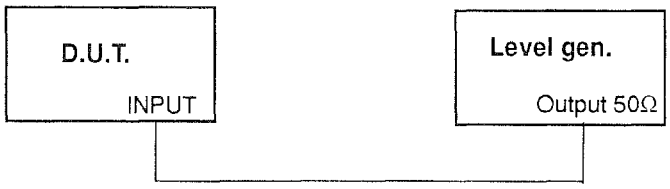


Fig. 8-6 Test setup for attenuator error

Instrument settings

Level generator: Z_0: 50 Ω
Frequency: 10 MHz
Level: -20 dBm

D.U.T.: PRESET, SPECTRUM ANALYSIS (CW)
FCENT: 10 MHz
FSPAN: 0 Hz
REFERENCE: -19 dBm
SCALE: 10 dB
RBW: 1 kHz
VBW: 10 Hz
SWT: 25 ms
ATTN: 10 dB
AUTO CAL: OFF

Measurement

Reference measurement:

Make a measurement using the above test setup and settings
Activate the ABS and REL markers (press "MKR" twice).
Use the MARKER TRANSF / ABS-->REF softkeys to set the line to the reference line.
Use the MARKER / MARKER UPDATE softkeys to set the ABS marker to HOLD.
The reference signal is now stored.

Attenuator measurement:

Set the input attenuator ATTN to the X values given in the table (use the arrow keys, except for 0 dB: "0" "ENTER") and compare the REL level displayed by the D.U.T with the specified error limits.

X (ATTN / dB)	0	10	20	30	40	50	60	65
Error limits (e) / dB	0.5	Ref.	1.1	0.6	0.9	2.0	1.5	2.0

8.7 Frequency Response

Equipment required

1 Synthesizer	TG-20 /-23	W&G
	or 83640	HP
1 Power Meter with	438A	HP
1 Power Sensor	8485A	HP
1 10 dB attenuator pad	8493C; Option 010	HP
1 Cable, 61 cm	11500 E	HP
1 Adapter PC3.5 for SNA	S896	W&G

Test setup

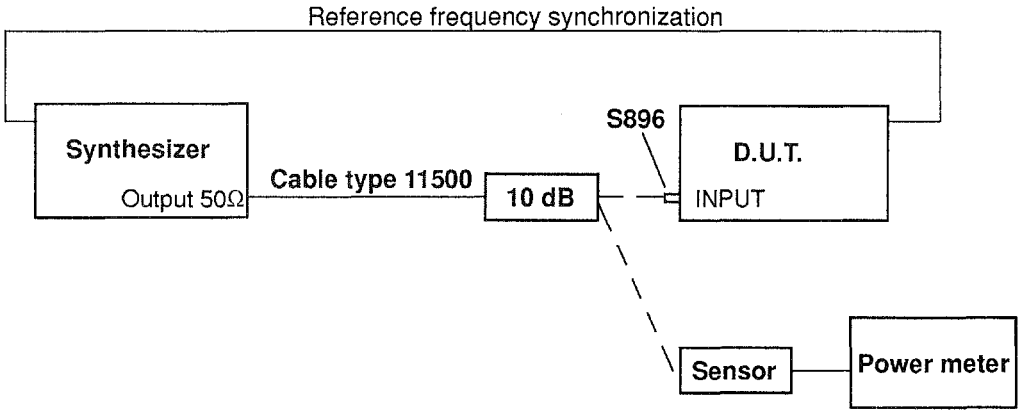


Fig. 8-7 Test setup for frequency response measurement

Instrument settings

Power Meter:	Mode:	dBm
Synthesizer:	FREQUENCY CENTER:	see f in table
	FREQUENCY SPAN:	0 Hz
	SWEEP:	SINGL
	POWER LEVEL:	approx. -7 dBm
D.U.T.:	PRESET, SPECTRUM ANALYSIS (CW)	
	FCENT:	see f in table
	FSPAN:	0 Hz
	REFERENCE:	-17 dBm
	SCALE:	10 dB
	RBW:	30 kHz
	VBW:	1 kHz
	SWT:	2 s
	ATTN:	10 dB

Test setup calibration

Before starting the measurement calibrate the Power Meter using its built in source and adjust the zero with no input level.
Perform external calibration of the D.U.T. and disable the internal automatic calibration (AUTO CAL = OFF).

Measurement

The frequency response measurement must be performed using PC 3.5 connectors!
Test setup as in figure 8-7; instrument settings as above.

Recording the reference values:
Connect the 10 dB attenuator pad directly to the Sensor (without adapter or cable).
Set the synthesizer to the measurement frequency (see table).
Enter the appropriate CAL. FACTOR for the Power Sensor in the Power Meter (use the average of intermediate values).
Execute a single calibration of the D.U.T. (EXECUTE SINGLE CAL).
Offset the synthesizer level so that the Power Sensor indicates -20 dBm ± 0.5 dB.
Note this level as P_{PS}.

Measuring the D.U.T.:
Now connect the 10 dB attenuator pad directly to the D.U.T. (without adapter or cable).
Set the D.U.T. to the measurement frequency (see table). Make the measurement and press "PEAK".
Use the MARKER TRANSF / ABS-->REF softkeys to set the line to the reference line.
Subtract the previously noted value P_{PS} with correct sign from the reference value for the D.U.T. and compare the result with the specified error limit.

Repeat the procedure starting from "Measurement" for each frequency f .
The measurement can be speeded up by first measuring the reference value P_{PS} for each of the frequencies and then testing the D.U.T.

f	Specified error limit(e)
50 MHz	± 0.5 dB
100 MHz	± 0.5 dB
1.5 GHz	± 0.5 dB
3.1 GHz	± 0.5 dB
3.2 GHz	± 2.3 dB
5.3 GHz	± 2.3 dB
7.4 GHz	± 2.3 dB
7.5 GHz	± 2.5 dB
11.2 GHz	± 2.5 dB
14.9 GHz	± 2.5 dB
15.1 GHz	± 2.8 dB
20.8 GHz	± 2.8 dB
22.0 GHz	± 2.8 dB
26.5 GHz	± 2.8 dB

Frequencies above 3.2 GHz apply to SNA-23 and SNA-33 only.

8.8 Resolution Bandwidths (RBW)

Equipment required

Synthesizer	SNA-20/23 with TG-20/23	W&G
	or 83640	HP

Test setup

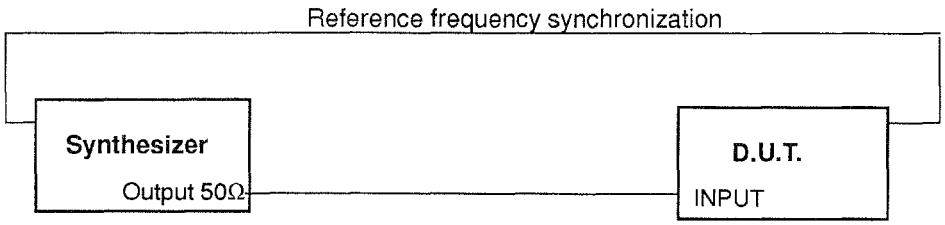


Fig. 8-8 Test setup for measuring the resolution bandwidths

Instrument settings

Synthesizer:	FREQUENCY:	100 MHz
	LEVEL:	-10 dBm
D.U.T.:	PRESET SPECTRUM ANALYSIS (CW)	
	FCENT:	100 MHz
	FSPAN:	see table
	REFERENCE:	-5 dBm
	SCALE:	10 dB
	RBW:	see table
	VBW:	100 Hz
	SWT:	see table
	ATTN:	10 dB

Measurement

Perform an internal calibration (using the CAL ; EXECUTE SINGLE CAL softkeys) before each measurement (after changing the RBW).

Set the D.U.T. as above, and select TRACE AVERAGE (using the TRACE; TRACE PROCESS softkeys).

Measurement of 3 dB bandwidth:
Activate the ABS marker and press "PEAK" (to measure the highest point on the filter curve). Activate the REL marker and move it to the lower edge with the rotary control until the level displayed is exactly -3 dB (for RBW = 10 MHz: -6 dB).
Note the frequency value . Now move the REL marker to the upper edge until the level displayed is exactly -3 dB (for RBW = 10 MHz: -6 dB). Compare the difference of the two frequency values with the maximum permitted difference [± B (3 dB)] stated in the table.

Measurement of 60 dB bandwidth:
Set SCALE = 100 dB. Then use the same procedure as for the 3 dB bandwidth to measure the 60 dB bandwidth.

The quotient B(60 dB) / B(3 dB) = Shape Factor (Sf) of the filter must not exceed the value Sf_{max} stated in the table.

Notes on the measurement:

- The 6 dB bandwidth is checked for RBW = 10 MHz.
- The 60 dB bandwidth (and thus Sf) cannot be measured for the SNA-20/-23 at RBW = 1 kHz, due to the phase noise of the D.U.T.
- It is normally sufficient to check the 3 kHz, 100 kHz and 10 MHz bandwidths.

RBW	VBW	FSPAN (3 dB / 60 dB)	SWT (3 dB / 60 dB)	± B (3 dB)	Sf_{max}
1 kHz	30 Hz	2 kHz / 20 kHz	5 s / 5 s	10%	11
3 kHz	100 Hz	6 kHz / 60 kHz	1 s / 1 s	10%	11
10 kHz	300 Hz	20 kHz / 200 kHz	1 s / 1 s	10%	11
30 kHz	1 kHz	60 kHz / 600 kHz	1 s / 1 s	10%	11
100 kHz	3 kHz	200 kHz / 2 MHz	1 s / 1 s	10%	11
300 kHz	10 kHz	600 kHz / 6 MHz	1 s / 1 s	10%	11
1 MHz	30 kHz	2 MHz / 20 MHz	1 s / 1 s	10%	11
2 MHz	100 kHz	6 MHz / 30 MHz	500 ms / 500 ms	10%	11
10 MHz	300 kHz	20 MHz / 50 MHz	500 ms / 500 ms	20% (6 dB)	3 (60 dB/6 dB)

"Narrow Filters" option, BN 2101/00.03

- The following RBWs can be set on the SNA-30/-33, and on the SNA-20/-23 if fitted with the "Narrow Filters" option, BN 2101/00.03. The 60 dB bandwidth (and thus Sf) cannot be measured for the SNA-20/-23 due to the phase noise of the D.U.T.
- The narrow bandwidths are software-generated using FFT. It is normally sufficient to checkjust one bandwidth (e.g. 300 Hz).

RBW	VBW	FSPAN (3 dB / 60 dB)	SWT (3 dB / 60 dB)	± B (3 dB)	Sf_{max}
300 Hz	10 Hz	600 Hz / 6 kHz	10 s / AUTO ON*	2%	10.2
100 Hz	3 Hz	200 Hz / 2 kHz	20 s / AUTO ON*	2%	10.2
30 Hz	3 Hz	60 Hz / 600 Hz	20 s / AUTO ON*	2%	10.2
10 Hz	3 Hz	20 Hz / 200 Hz	20 s / AUTO ON*	2%	10.2
3 Hz	3 Hz	6 Hz / 60 Hz	20 s / AUTO ON*	2%	10.2
1 Hz	3 Hz	2 Hz / 20 Hz	50 s / AUTO ON**	2%	10.2

* = 33.3 s ** = 100 s

8.9 Intrinsic Spurious Signals without Input Signal

8.9.1 Intrinsic Noise

Equipment required

1 terminating resistor 50 Ω 909D HP

Test setup

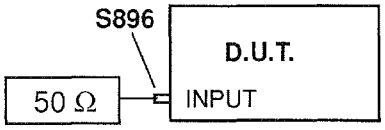


Fig. 8-9 Test setup for measuring intrinsic noise

Instrument settings

D.U.T.: PRESET, SPECTRUM ANALYSIS (CW)
FCENT: see table
FSPAN: 0 Hz
REFERENCE: -60 dBm
RBW: 1 kHz
VBW: 10 Hz
SWT: 100 ms
ATTN: 0 dB

Measurement

Set the D.U.T. as above and select TRACE AVERAGE (using the TRACE; TRACE PROCESS softkeys).
After about 5 sweeps (averages) press "PEAK" and compare the level value of the ABS marker with the corresponding typical value in the table.
Press "PEAK" again each time FCENT is changed to update the level value.

FCENT	ABS (typical)
99.9 MHz	-127 dBm
999.9 MHz	-127 dBm
2.999 GHz	-124 dBm
13.999 GHz	-118 dBm
22.999 GHz	-115 dBm
26.499 GHz	-108 dBm

8.9.2 Discrete Spurious Signals

For equipment required and test setup, see chapter 8.9.1.

Instrument settings

D.U.T.: PRESET, SPECTRUM ANALYSIS (CW)
FCENT: see table
FSPAN: 10 kHz
REFERENCE: -60 dBm
RBW: 1 kHz
VBW: 100 Hz
SWT: AUTO ON (500 ms)
ATTN: 0 dB
TRACE PROCESS:AVERAGE

Make the settings given in the table and use the PEAK function to hold the level maximum after at least 5 sweeps. Compare the measured value with the corresponding typical value in the table.

FCENT	ABS (typical)
16 MHz	-110 dBm
20.209 MHz	-110 dBm
421.99 MHz	-110 dBm
631.7128571 MHz	-110 dBm
1.789005 GHz	-110 dBm
3.367015 GHz	-105 dBm
4.42199 GHz	-105 dBm
5.2 GHz	-105 dBm
11.2 GHz	-100 dBm
12.8 GHz	-100 dBm
14.8 GHz	-100 dBm

Frequencies above 3.2 GHz apply to SNA-23 and SNA-33 only.

8.10 Additional Tests

The following additional tests are not part of a normal check.
It will not normally be necessary to perform these tests.
Some tests require a large quantity of measuring equipment.

8.10.1 Intrinsic Spurious Signals with Input Signal

8.10.1.1 Harmonic Attenuation

Equipment required

1 Synthesizer (up to 1.6 GHz)	SNA-20/ -23 with TG-20/ -23 or 83640	W&G HP
1 Low-pass filter f_{lim} = 900 MHz	Type 2001.17F	Suhner
1 Low-pass filter f_{lim} = 1400 MHz	Type 2001.17G	Suhner
1 Low-pass filter f_{lim} = 2100 MHz	Type 2001.17B	Suhner

Test setup

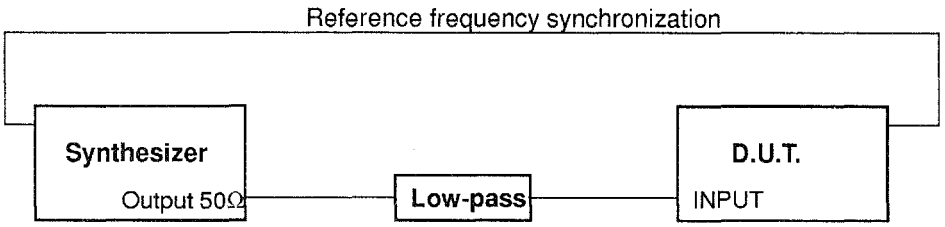


Fig. 8-10 Test setup for harmonic attenuation

Instrument settings

Synthesizer:
FCENT: = f_{meas}
FSPAN: 0 Hz
SEND LEVEL: -30 dBm

D.U.T.:
PRESET, SPECTRUM ANALYSIS (CW)
FCENT: f_{meas}, 2 x f_{meas}, 3 x f_{meas}
FSPAN: 0 Hz
REFERENCE: -25 dBm
SCALE: 100 dB
RBW: 1 kHz
VBW: 10 Hz
SWT: 100 ms
ATTN: 10 dB
TRACE AVERAGE (select using TRACE; TRACE PROCESS softkeys).

Technical note

The harmonic attenuation values are very dependent on the Q of the low-pass filters used.

Measurement (a_{k2})

Reference measurement:
Externally calibrate the D.U.T.
Set the desired fundamental f_{meas} for the generator and the D.U.T..
Activate the ABS and REL markers (press "MKR" twice).
Adjust the synthesizer level so that the D.U.T. displays -30 dBm.
Use the MARKER TRANSF / ABS-->REF softkeys to set the level to the reference line.
Use the MARKER / MARKER UPDATE softkeys to set the ABS marker to HOLD.
The reference value is now stored.

Measuring a_{k2}:
Set the D.U.T. to FCENT = 2 f_{meas} .
The level value of the REL marker gives the harmonic attenuation. Compare this value with the corresponding value in the table below.

f_{meas}	$2f_{meas}$	Low-pass filter	a_{k2} (typical)
500 MHz 700 MHz	1000 MHz 1400 MHz	900 MHz 900 MHz	75 dB 75 dB
900 MHz 1200 MHz	1800 MHz 2400 MHz	1400 MHz 1400 MHz	75 dB 75 dB
1400 MHz 1600 MHz	2800 MHz 3200 MHz	2100 MHz 2100 MHz	75 dB 75 dB

Measurement (a_{k3})

Reference measurement:
Use the same procedure as for a_{k2}.

Measuring a_{k3}:
Set the D.U.T. to ATTN = 0 dB (mixer level -30 dBm) and FCENT = 3 f_{meas}.
The level value of the REL marker gives the harmonic attenuation. Compare this value with the corresponding value in the table below.

f_{meas}	$3f_{meas}$	Low-pass filter	a_{k3} (typical)
500 MHz 750 MHz 1 GHz	1.5 GHz 2.25 GHz 3 GHz	900 MHz 900 MHz 1400 MHz	70 dB 70 dB 70 dB

8.10.1.2 Sideband Noise Power Level

Equipment required

1 level generator	PSM-39	W&G

Test setup

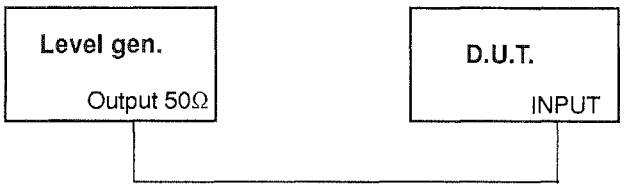


Fig. 8-11 Test setup for measuring sideband noise power

Instrument settings

Level generator: Z_0: 50 Ω
Frequency: 10 MHz
Level: -20 dBm

D.U.T.: PRESET, SPECTRUM ANALYSIS (CW)
FCENT: 10,005 MHz
FSPAN: 11 kHz
REFERENCE: +10 dBm
SCALE: 100 dB
RBW: 1 kHz
VBW: 30 Hz
SWT: AUTO ON
ATTN: 20 dB
TRACE AVERAGE (select using TRACE; TRACE PROCESS softkeys).
"dBm/Hz" (select via DISPLAY/ LEVEL/ UNITS)

Measurement

The sideband noise power level is measured at a spacing of 10 kHz from the carrier.

Make the settings as above.
Activate the ABS marker and press "PEAK" to measure the carrier peak value.
Use the MARKER TRANSF / ABS-->REF softkeys to set the level to the reference line.
Activate the REL marker and set it to +10 kHz.

After at least 5 sweeps (averages) compare the REL marker level value with the following value:

SNA-20/-23: typically -93 dBc/Hz
SNA-30/-33: typically -108 dBc/Hz

8.10.1.3 Intermodulation Attenuation

Equipment required

1 Synthesizer 1	SNA-20/-23 with TG-20/-23	W&G
	or 83640	HP
1 Synthesizer 2	83640	HP
1 Power Splitter	Type 1870A	Weinschel
2 10 dB attenuator pads	Type 44	Weinschel
1 Low-pass filter f_{lim}:14 MHz	0987-6500.324	W&G
1 Z_0 matching pad 50 Ω<->75 Ω	ZA 5075	W&G
1 Directional coupler	Type no. 4227-16	NARDA
1 Attenuator pad	4138060000	Radiall
2 Isolators	Type no. 4914	NARDA
2 Isolators	Type no. 4946	NARDA

Checking Band 0

Test setup

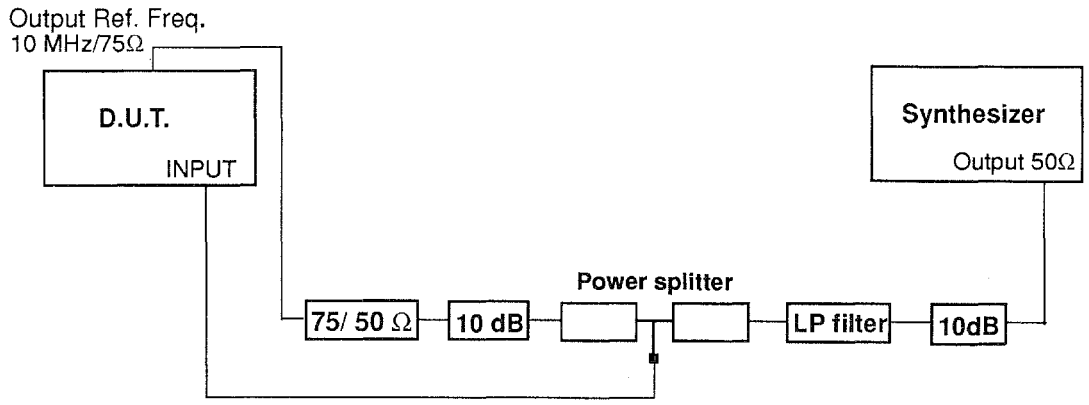


Fig. 8-12 Test setup for intermodulation attenuation, Band 0

Instrument settings for Band 0

Synthesizer:	Frequency:	10,1 MHz
	Level:	-2 dBm
D.U.T.:	PRESET, SPECTRUM ANALYSIS (CW)	
	FCENT:	10 MHz
	FSPAN:	50 kHz
	REFERENCE:	-15 dBm
	RBW:	AUTO ON
	VBW:	AUTO ON
	SWT:	AUTO ON
	ATTN:	**10 dB**

Seting the reference level

Test setup and settings as described above.
Activate the ABS marker and set it to the maximum of the 10 MHz signal (press PEAK)
Use the MARKER TRANSF / ABS-->REF to set the trace maximum at 10 MHz to the reference line.

Use the MARKER / MARKER UPDATE softkeys to set the ABS marker to HOLD.
Note the level value of the ABS marker as "X_1".
Set the REL marker to +100 kHz (10.1 MHz).
Now adjust the synthesizer level so that the REL marker level displays 0 dB.

Measurement

D.U.T.:	FCENT:	10.2 MHz
	VBW:	100 Hz

Select TRACE AVERAGE (using the TRACE; TRACE PROCESS softkeys).
Set the REL marker to +200 kHz (10.2 MHz).
Note the level value of the ABS marker as "X_2".
-> X_2 should typically be less than -30 + (2 X_1).

D.U.T.:	FCENT:	9.9 MHz

Note the level value of the ABS marker as "X_3".
-> X_3 should typically be less than -30 + (2 X_1).

Example:

X_1 = -20 dBm
-> X_2 or X_3 = < -30 + (2 x -20 dBm) = < -70 dB

Checking Bands1,2 and 3 (SNA-23/-33 only)

Test setup

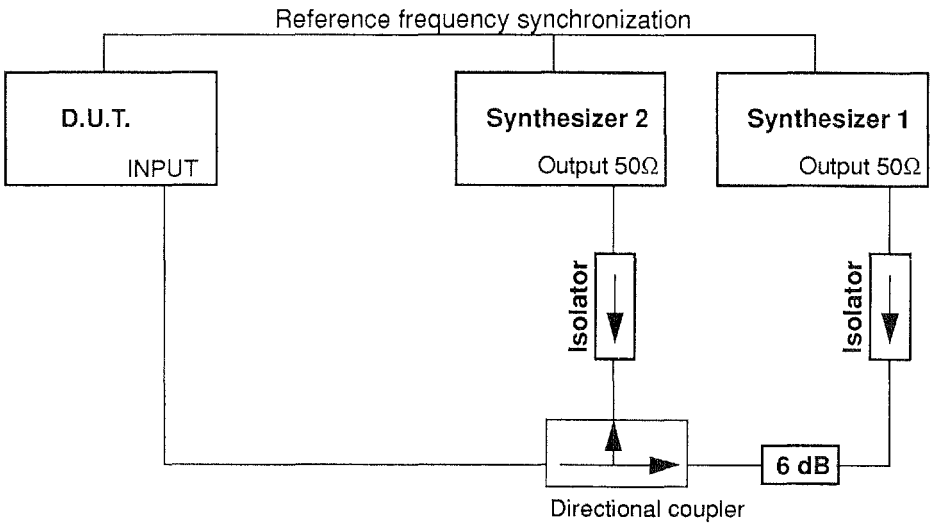


Fig. 8-13 Test setup for intermodulation attenuation, Bands 1, 2, 3

Instrument settings for Bands 1, 2, 3

Synthesizer 1:	Frequency:	see table
	Send level:	0 dBm
Synthesizer 2:	Frequency:	see table
	Send level:	8 dBm
Power Meter:	Mode:	dBm
D.U.T.:	PRESET, SPECTRUM ANALYSIS (CW)	
	FCENT:	see table
	FSPAN:	20 kHz
	REFERENCE:	-10 dBm
	SCALE:	100 dB
	RBW:	AUTO ON (1 kHz)
	VBW:	100 Hz
	SWT:	AUTO ON (1 s)
	ATTN:	10 dB

Test setup calibration

Externally calibrate the D.U.T..

Setting the reference level

Test setup and settings as described above.
Set the D.U.T. to FCENT = $F_{Synthesizer\ 1}$.
Set synthesizer 2 to "SEND LEVEL OFF" and adjust synthesizer 1 to give a D.U.T. receive level of -10 dBm 0.2 dB.
Activate the ABS marker and set it to the maximum of the signal (press PEAK).
Use the MARKER TRANSF / ABS-->REF to set the trace maximum to the reference line.
Use the MARKER / MARKER UPDATE softkeys to set the ABS marker to HOLD.

Set synthesizer 2 to "SEND LEVEL ON" and set the D.U.T. to FCENT = $F_{Synthesizer\ 2}$.
Set the REL marker to +100 kHz ($F_{Synthesizer\ 2}$).
Now set the level of synthesizer 2 so that the REL marker displays 0 dB.

Measurement

D.U.T.: TRACE AVERAGE
FCENT: see table

After at least 5 sweeps, use the HIGHEST PEAK marker function to set the REL marker to the trace maximum.
Note the level value of the REL marker as X.

F Synthesizer 1	F Synthesizer 2	FCENT D.U.T.	Isolator
6.0001 GHz 11.0001 GHz 18.0001 GHz	6.0002 GHz 11.0002 GHz 18.0002 GHz	6 GHz and 6.0003 GHz 11 GHz and 11.0003 GHz 18 GHz and 18.0003 GHz	No. 4914 No. 4946 No. 4946

Nominal value of X: typically >70 dB.

8.10.2 Checking the Return Loss

Equipment required

1 Scalar network analyzer	8757E	HP
1 Synthesizer	83640A	HP
1 Return loss bridge with standards	85027B	HP

Test setup

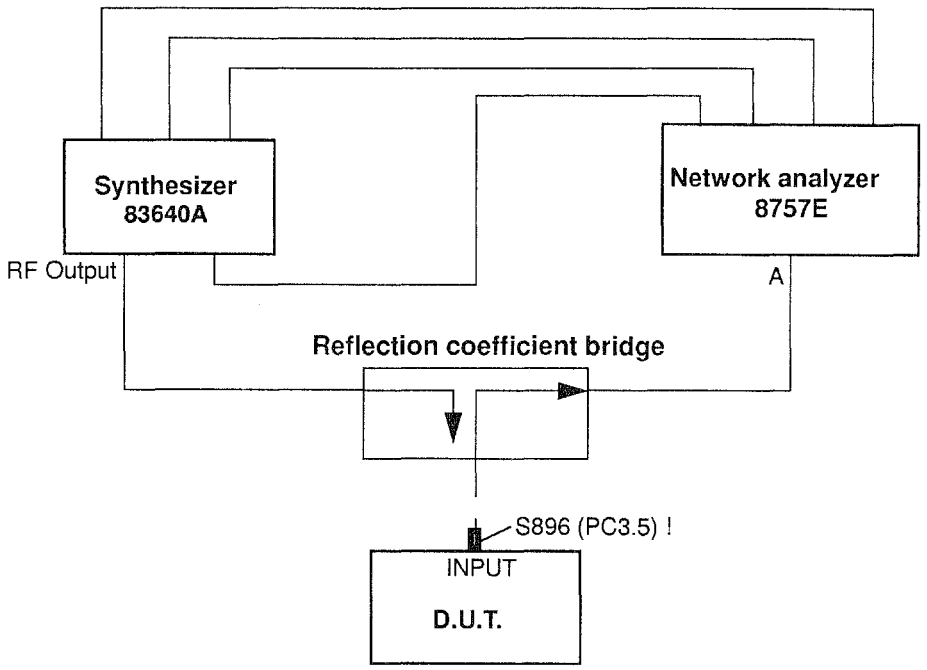


Fig. 8-14 Test setup for measuring return loss

Instrument settings

Network analyzer and synthesizer:

	PRESET	
	CHAN2:	OFF
	SCALE:	5 dB
	START FREQUENCY:	see table
	STOP FREQUENCY:	see table
D.U.T.:	PRESET, SPECTRUM ANALYSIS (CW)	
	FCENT:	2 GHZ (4 GHz)
	FSPAN:	0 Hz
	REFERENCE:	-20 dBm
	ATTN:	10 dB
	other settings:	AUTO ON

Test setup calibration

Calibrate the test port of the reflectometer bridge in short- and open-circuit using the CAL function of the network analyzer (refer to the operating instructions for these instruments).

Measurement

Connect the test port of the reflectometer bridge directly to the input of the D.U.T. Now read off the maximum displayed value on the network analyzer using the cursor function. Compare the magnitude of this value with the specified error limit given in the table.

FCENT D.U.T.	Frequency range, synthesizer	Typical return loss value	Note
2 GHz	10 - 3200 MHz	20 dB	
4 GHz	3200 - 12400 MHz	15 dB	for SNA-23/-33 only
4 GHz	12400 - 26500 MHz	12 dB	for SNA-23/-33 only

9 Function and circuit description, SNA-20/-23

9.1 Description of complete instrument function

In the following description, it is assumed that the Description and Operating Manual has been read and understood. The descriptions refer to the block circuit diagram located in the Annex to this Service Manual.

The descriptions refer to the SNA-23 but may be considered as applying also to the SNA-20, since the instruments are practically identical. The only difference is that the signal path for Bands 1, 2 and 3 is not present in the SNA-20, i.e. the circuits (3) YIG filter control and (4) fundamental mixer are not fitted. The instruments are practically identical for Band 0.

The SNA-20/-23 comprises the following function groups:

- Frequency converter
- IF measurement section
- Synthesizer
- Controller
- AC power supply unit

9.2 Frequency converter, input section BN 2101 (2), (3), (4), (5), (6)

In the input section, the measurement signal at the input socket is converted to an intermediate frequency of 422 MHz (421.99 MHz) by single or double mixing and passed on to the IF modules after amplification (compare block diagram in Appendix).
When the instrument is set to frequencies between 9 kHz and 3.2 GHz (Band 0 operation), the input signal first passes through the step attenuator and is then fed from the coaxial switch (replaced from series C by the diplexer 2DX1) via the 7 GHz coaxial low-pass filter to the Band 0 frequency converter (2) [2101-ZA] (Integration Band 0) microwave module.
The first frequency conversion to the IF (above the Band 0 frequency range) of 4.422 GHz (4.42199 GHz). The heterodyne signal required for this is supplied by the synthesizer OD-11 and fed in via the fundamental mixer module in the input section. The input mixer is protected against impermissibly high RF drive levels by limiter diodes.
The IF signal next passes through a combination of filter and amplifier, which filters out the remains of the carrier signal and unwanted mixer products and amplifies the signal level such that the following second mixer is optimally driven.
This mixer requires a carrier signal with a fixed frequency of 4 GHz in order to convert to the second IF of 422 MHz. The 4 GHz heterodyne signal is generated by locking a voltage-controlled oscillator to harmonics of the 400 MHz reference frequency from synthesizer OD-11.
When the instrument is set to input frequencies from 3.1 to 26.5 GHz (Band 1 to 3 operation), the 422 MHz IF signal is generated from the input signal at the input socket using a different method.
In this case, the coaxial switch (diplexer from series C) feeds the input signal to the YIG filter. The center frequency of this bandpass filter can be tuned in the range 3 to 26.5 GHz (30 GHz) by means of a DC voltage. Controlled from the "YIG filter controller" board, it is synchronized to the actual receive frequency of the instrument and serves to suppress image frequencies, because single conversion directly to the 422 MHz IF is used for bands 1 to 3.
The circuitry required for this frequency conversion is contained in the fundamental mixer microwave module.
A broadband mixer circuit converts the input signal directly to 422 MHz with relatively low losses of about 10 dB. The is fed on the LO side by a carrier signal which has a frequency of one, two or four times the synthesizer frequency, depending on the input frequency range (band). The

output frequency of the YIG oscillator (OD-11) is multiplied for this purpose by a combination of amplifiers, switches and doublers in the fundamental mixer.
The module also provides an output of the simple YIG oscillator frequency for the Band 0 frequency converter (Integration Band 0) module [2101-ZA] and for the back panel socket for connection to a tracking generator or external mixer.
The 422 MHz IF switch module (2) [2101-AQ1] takes the IF signal from the Integration Band 0 module or from the fundamental mixer and equalizes the level differences for the different paths. A third path is provided here for directly feeding in an external measurement signal of 422 MHz (e.g from an external mixer).
The amplified IF signal leaves the input section chassis with a nominal level of approx. -33 dBm (Band 0) and is then fed to the 422 MHz bandpass filter (interdigital filter (6) IF-1) in the "422/ 22 MHz converter" module. The 422 MHz IF signal is converted here to the last IF (21.99 MHz).
The various switching states of the input section modules are controlled by the input section controller board via the peripheral bus (AT CPU). Depending on the different instrument operating modes, the bus information is processed on this circuit board so as to keep the circuitry needed in the microwave modules to the minimum

9.2.1 Input section controller (5) [2101-AR]

The input section controller board is the central supply and control circuit for the input section chassis. The various DC voltages from the AC PSU are fed to the microwave and IF modules via this circuit board, being pre-filtered if necessary. Only the YIG filter controller board is connected directly by its own cable to the AC PSU.
The main task of the "input section controller" is, however, the conditioning of the digital control signals from the peripheral bus for direct control of the microwave components of the input section.
The information is written from the bus data lines (8 bits) to a LSI module (PIO, U11) or written from the PIO to the bus data lines when addresses in the range specified for the input section are also present on the address lines.
The following control functions are realized on the "input section controller" board:

- **PIO Port 0:** Intermediate storage and loop-through of data for the YIG filter controller (3) [2101-AS1] including the associated control logic.
- **PIO Port 1:** Intermediate storage and conditioning of the control signals for band switching (coaxial relay, 422 MHz IF switch, Integration Band 0 module and fundamental mixer) as well as for Signal Identifier operating mode (VCO 400/402 MHz).
- **PIO Port 2:** Intermediate storage of a data word and conversion to a (bipolar) DC voltage for setting the working point of an externally-connected mixer via the 422 MHz IF switch.
- **PIO Port 3:** Intermediate storage of the data word for controlling the step attenuator including level conversion.
- **PIO Port 4:** Transfer of register contents towards the CPU depending on the address, either from the output register of the YIG filter controller or from the error register of the input section controller (which contains information about the operating status of the microwave modules) or from the input section control status register (in which bit 0 indicates error states in the input section).

9.2.2 Frequency converter band 0 (2) [2101-ZA] (Integration Band 0)

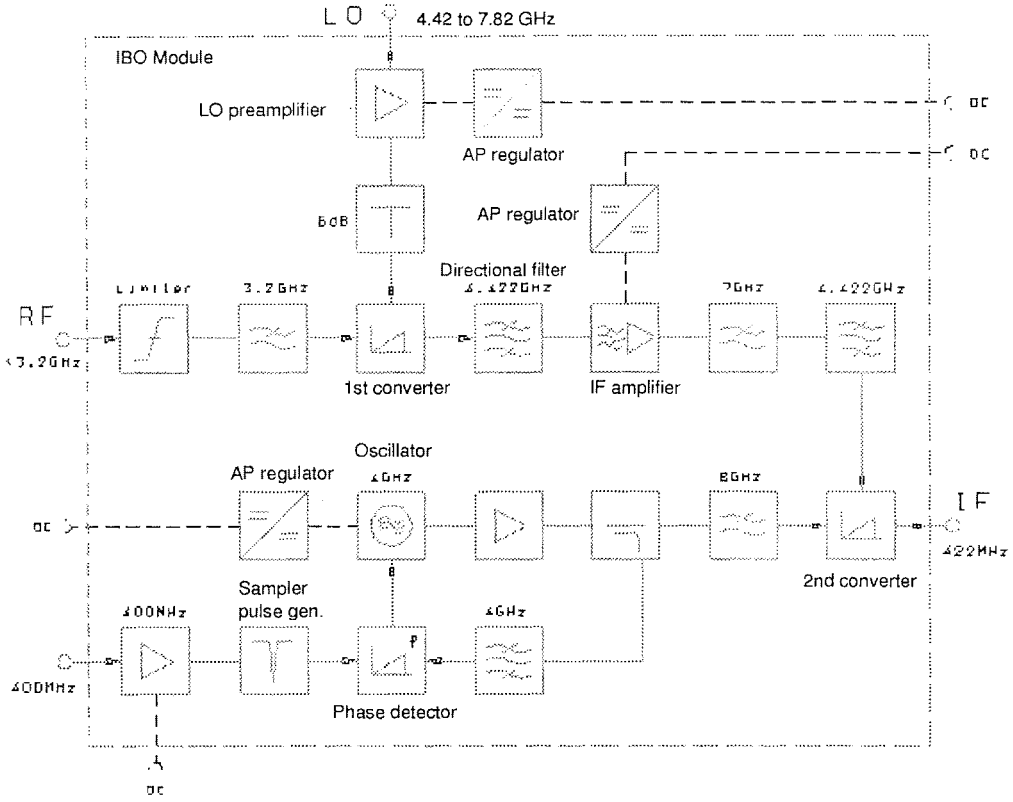


Fig. 9-1 "Frequency converter Band 0" microwave module [2101-ZA] block diagram

A limiter, comprising two PIN diodes connected in antiparallel at the input of the module, protects the first converter from input signals which are too high (max. 1 W RF power). The subsequent low-pass filter suppresses the LO signal and its image frequencies which are travelling back towards the input socket (RF input).
The first converter is a simple push-pull converter which uses the LO signal to convert the input signal to the 1st IF of 4.422 GHz. The subsequent directional filter provides wideband termination for the converter. The input LO signal (4.42 to 7.82 GHz) is amplified to approx. 23 dB by the LO amplifier.
The 1st IF signal is amplified by 16 dB by the two-stage selective IF amplifier and is then fed to a filter combination of a low-pass and a bandpass filter with a bandwidth of b_{5dB} = 3.5%. The subsequent 2nd converter uses a 4 GHz carrier to convert the 1st IF (4.422 GHz) to the 2nd IF (422 MHz) which exits from the module via the IF output. The mixer losses are about 4 dB.
The oscillator (VCO) generates the LO frequency (4 GHz) required for the 2nd conversion. The 4 GHz signal is frequency-locked to a 400 MHz signal derived from the timebase.
The 4 GHz signal is fed to the VCO low-pass filter via the amplifier and the directional coupler. The output power level is 13 to 16 dBm. The VCO low-pass filter (f_g = 8.2 GHz) suppresses the high-frequency components in the carrier which must not get into the second converter.
A 400 MHz signal derived from the timebase is fed into the module, amplified by the driver amplifier and is used to control the pulse sampler. The pulses generated are fed to the sampling mixer which is used as a phase meter. The 4 GHz signal from the oscillator which is coupled out by the directional coupler is fed via the 4 GHz band-pass filter to the phase meter. The mixer

product thus generated in the locked state is a DC voltage which is fed to a PLL integrator. The working point regulators for the amplifier are thick film circuits. They are PI regulators and guarantee that the gates of the RF transistors are negatively-biased in all operating states.

9.2.2.1 Integration Band 0 controller (2) [2101-CF]

The Integration Band 0 controller board performs the following tasks:

- Voltage filter
- PLL integrator and seek circuit
- Band 0 switch-off
- Voltage stabilization
- Working point control
- Error signal generation

Voltage filter

AC voltages which may be superimposed on the ± 12 V supply voltages are removed by the filters L1 through L4, C16 through C19 and C34, C35. Low-frequency interference is filtered out by the components around transistors Q5 or Q8. Transistor Q6 switches the negative supply voltage off if the positive supply voltage fails.

PLL integrator and seek circuit

The phase detector output signal is fed to the board via sockets J1 and J2. This signal contains the phase difference between the 400 MHz signal and the 4 GHz signal and is a DC voltage in the locked state. If not locked, a beat frequency is present at the output of impedance converter U1, which causes the signal comparator U5 to trigger the monostable U6.1 which then supplies an output voltage of 5 V. This causes the seek oscillator U3 to oscillate at f_{osc} = 80 Hz. This generates a sawtooth tuning voltage (J3) for the VCO varactor (VCO TUNING VOLTAGE). R54 is used to adjust the tuning voltage in the locked state.

Band 0 switch off

When the instrument is tuned in the higher receive frequency bands, the 4 GHz carrier must be switched off. The VCO is disabled by a voltage of 0 V at MP10.8, shorting out the VCO oscillator transistor. The VCO settles within approx. 20 ms when switched on again (MP10.8: 5 V).

Voltage stabilization

A stabilized +5 V supply voltage is required for the hybrid working point controller on the module (J6 and J7). This voltage must be controlled so that it is only switched through to the RF circuits when the negative supply voltage (-11.2 V) is present. This protects the RF amplifier (self-conducting FETs) from damage.

Working point controller

The working point controller for the 400 MHz amplifier is made up from operational amplifier U4 and transistor Q4.

Error signal generation

The +5 V supply voltage for the hybrid working point controller is protected using a foldback current limiter. At the same time, the voltage is compared with a reference value. If it is below the reference value, an error signal (MP10.9) is generated and LED DS3 lights up.
If the VCO is not locked, the integrator output voltage U2 tends towards ± 11 V and the window discriminator U7 generates a further error signal (MP10.10) causing LED DS1 to light up.

9.2.3 YIG filter control (3) [2101-AS1]

The YIG filter (FL1) serves as a preselector for bands 1, 2 and 3 at the input of the instrument. The main job of the YIG filter is to suppress image frequencies, harmonic and all interference signals which are not close to the measurement frequency. The YIG filter is a magnetic field-dependent microwave bandpass filter. The filter is tuned using an very precisely controlled current through the COIL connections of the filter (magnetic field).
The YIG filter controller (3) has the task of providing this tuning current for the YIG filter for the entire tuning range (3 to 30 GHz) with the necessary precision. As the relationship between tuning frequency and tuning current is non-linear, the characteristics of each filter must be measured and stored (in Flash EPROMs). The characteristic is then taken into account when controlling the YIG filter during measurement operation.

The YIG filter control comprises several function groups:

- Microcontroller unit (MCU)
- State controller (function decoder)
- Memory (FIFO)
- CPU latch
- Synthesizer latch
- Hardware summing circuit (adder)
- Flash EPROMs
- DAC latch
- Precision reference
- Precision DAC
- V/I converter
- YIG filter heater voltage

Apart from the above function groups, other functions are built in to the YIG filter controller board. To preserve clarity, these are not shown in the simplified block diagram. They include:

- Generation of the Flash EPROM programming voltage
- Temperature sensor
- Supply voltage filters, etc.

The tasks and functions of the individual units are described with the aid of the simplified block diagram (see figure 9-2).

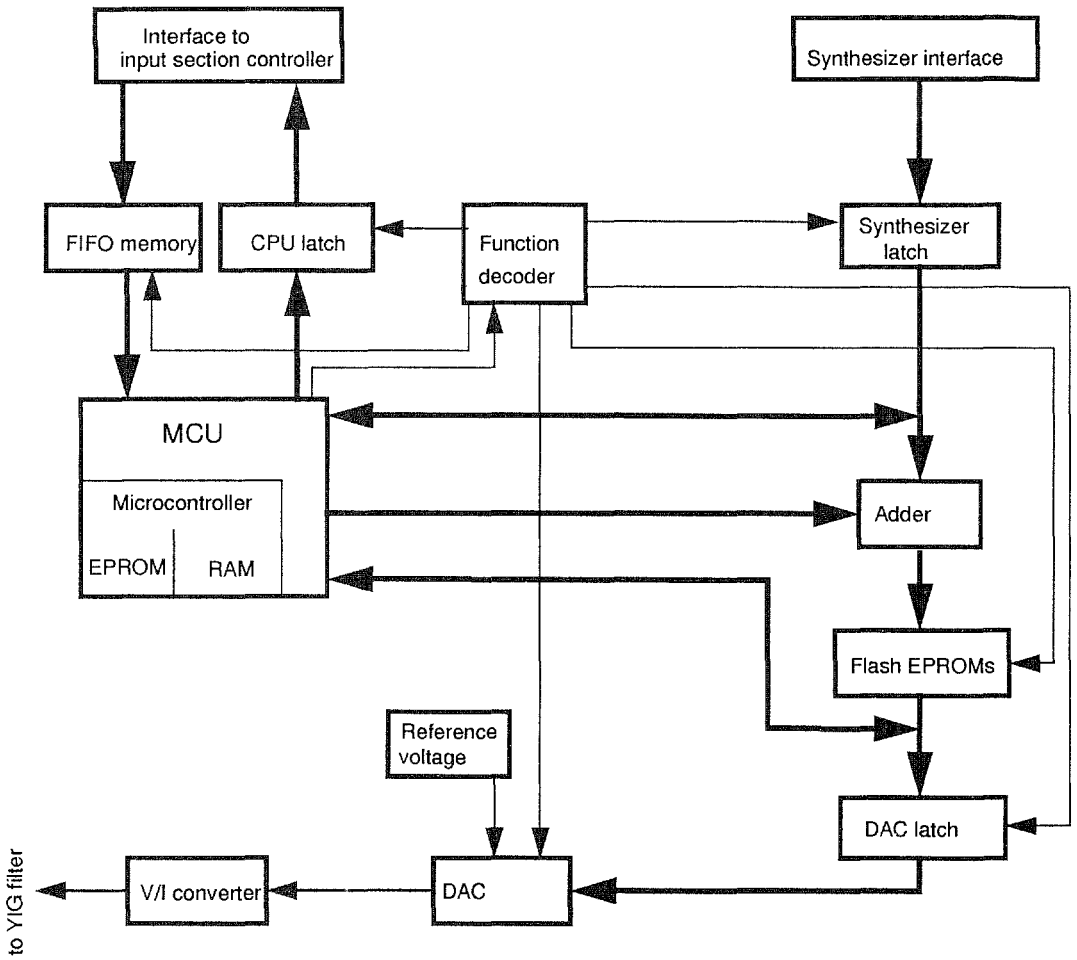


Fig. 9-2 YIG filter controller (3) simplified block diagram

Microcontroller unit (MCU)

The SIEMENS 8-bit microcontroller SAB80C537 (U29) is used. The microcontroller has an external program memory (U27) and external RAM (U31). The MCU independently controls all processes in the **Y**IG **f**ilter **c**ontroller (YFC). For this, it receives commands from the control computer (AT-CPU) which are transferred via the input section controller/FIFO memory. The frequency information is supplied to the MCU by the synthesizer controller (51).

State controller (function decoder)

The state controller manages all path states, i.e. the operating direction of bidirectional buffers, the port enables for the output drivers and the switching of functions (e.g. program voltage to the Flash EPROMs).
The MCU uses 4 control lines to control the states (P0 through P3). Two completely different types of state can be set in this way:

- permanent states (Y0 to 7)
- transition states (Y8 to 15)

All states are indicated by LEDs, so that each change of state can be followed visually (see "Function decoder" circuit in circuit diagrams).

FIFO memory

The data transfer from the control computer (via the input section controller) to the YIG filter controller is processed via the FIFO memory U30. The FIFO memory (U30) is 64 x 9bit deep and is coupled directly to the MCU via port P7. This allows the FIFO to be read in any operational state. The input section controller and the control computer can only detect overflow of the FIFO by monitoring the number of bytes written but not yet acknowledged. Line SI is supplied by the input section controller, i.e. is decoupled from the YIG filter controller logic. This makes the write operation completely independent of the read operation by the YIG filter controller.

CPU latch

The data are passed via (U26) from the YIG filter controller to the control computer (via the input section controller). The data transfer is triggered by state (Y10). The latch enable input is served from the control computer via the input section controller. An automatic lock-up prevents new data from being loaded into the latch when the latch output is enabled (write access lock).
The CPU latch (U26) is written to via the C/F data channel which also transfers the frequency addresses (lower byte) between the MCU and the synthesizer EPROM path. The path to the frequency addresses (FR (15:0)) is disconnected via U16 by (Y2; function decoder) for operation of the CPU latch.
The value on P3.4 (C/F8) is written to the error register (U22.1) at the same time as writing to the CPU latch. The is passed directly to the error interrupt (and linked to other error circuits via the input section controller). This allows fatal errors to be indicated to the control computer.

Synthesizer latch

The data provided by the synthesizer (frequency information) is latched by U1 and U2, i.e. the current frequency of the synthesizer is always available at this point. If, in the meantime, a different value is set on the frequency addresses (FR (15:0)), e.g. by the MCU, or if the YIG filter is disabled in the meantime, the YIG filter can be set to the latest valid frequency value at any time by reading the data from the synthesizer latch. Storage in the latch is triggered by the strobe from the synthesizer, without being affected by the YIG filter controller.

Hardware summing circuit (adder)

Here, offset values are simply added to the frequency word coming from the synthesizer or from the MCU itself. The adder operates purely on a hardware basis without any functional control by the MCU.

Flash EPROMs

The Flash EPROMs store the characteristics of the YIG filter, outputting a corresponding code for every value to which the synthesizer can be set (frequency information). The conversion of this code by the DAC (U42) and subsequent V/I conversion produces the YIG filter setting current. This guarantees that the pass-band of the YIG filter is correctly set for every input frequency (synthesizer frequency).
The hardware required for programming (program voltage generator) is included in the circuit (U39.1, U25.1, Q1). Programming is done by the MCU without removal of the Flash EPROMs.

DAC latch

The output data from the characteristics Flash EPROMs is buffered by latches (U12, U13) and fed from these to the DAC (U42).

Precision reference

The voltage reference is produced using a thermally-controlled regulator diode (U44) and external reference elements. This ensures the excellent thermal stability required for the reference voltage.

Precision DAC

The DAC (U42; AD 7846) used is a 16-bit device with voltage output and high thermal constancy. The excellent thermal stability required for correctly controlling the YIG filter in the entire nominal operating temperature range is achieved in conjunction with the precision reference (reference voltage generator).

V/I converter

The output voltage from the DAC corresponding to the YIG filter characteristic is converted into the corresponding current for controlling the YIG filter (current interface J21; approx. 0 to 1 A).

YIG filter heater voltage

The heater voltage is available from P11, pins P11.1 and P11.3. This is limited to a maximum of approx. 0.5 A by U46 (LM317).

9.2.4 Fundamental mixer (4) [2101-ZC]

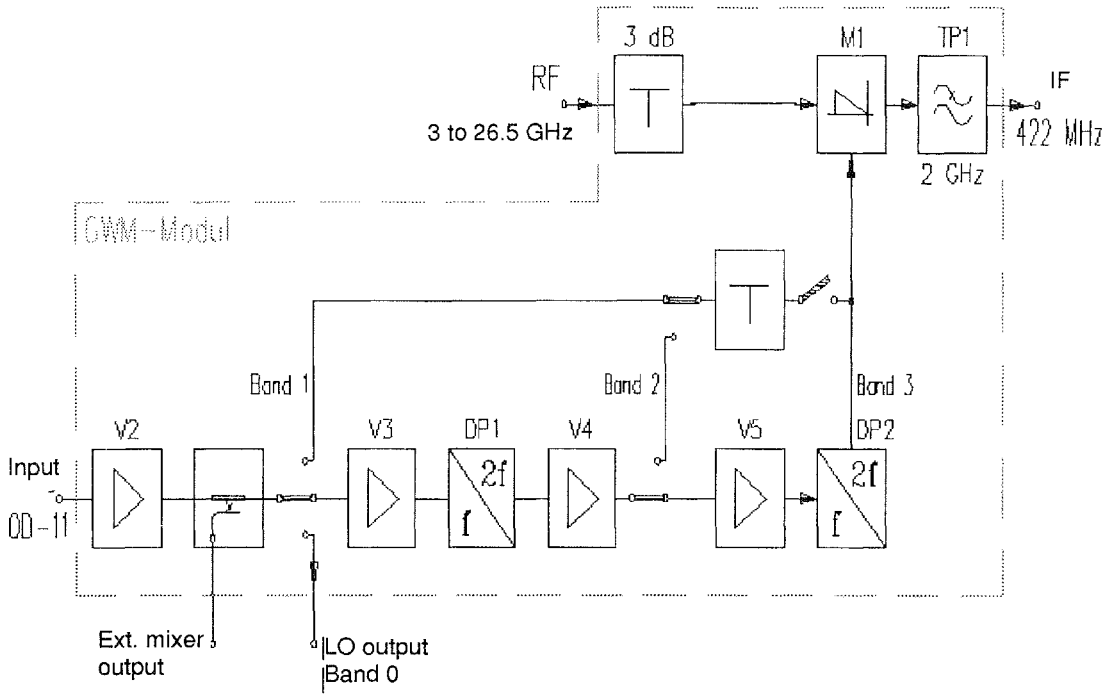


Fig. 9-3 Fundamental mixer [2101-ZC] block diagram

The microwave module contains a mixer stage with low-pass filter and carrier frequency conditioning.
The high frequency RF input signal passes through an attenuator (3 dB) to improve the input reflection coefficient. The push-pull mixer stage M1 is controlled by a carrier spaced at f_{IF} = 422 MHz above the input frequency f_{RF}. This converts the RF signal to a constant, low-frequency IF of422 MHz. A low-pass filter TP1 leads to the module's IF output.
The carrier frequency conditioning raises the synthesizer signal (OD-11) to an approximately constant level and limits it. This signal is then either passed on directly to the mixer stage M1 (Band 1) or multiplied by switching in frequency doubler stages (Band 2 and 3) before it is fed to the mixer stage.
For controlling the separate input section in Band 0, the carrier signal can be switched to an output (LO output Band 0). The carrier signal is also available from a further output as a local oscillator for control of an external mixer.

9.2.4.1 Fundamental mixer controller (4) [2101-AV1]

The fundamental mixer controller performs the following tasks:

- Voltage stabilization
- Error signal generation
- Working point regulation
- Band switching

Voltage stabilization

Several voltage stabilizer circuits are fitted to this board.
Voltages of +10 V and -10 V are also generated for the band switching.

Error signal generation

The +5 V voltage is protected using a foldback current limiter. At the same time, the voltage is compared with a reference value. If it is below the reference value, an error signal is generated at MP2.4 (open collector).

Working point regulators

The working point regulators for amplifiers V2 and V3 are thick-film modules in the RF circuits. The circuits guarantee that the gates of the RF transistors are negatively-biased in all operating states.

Band switching

The band information is available as a 2-bit data word at MP 2.1 and MP 2.2. Control voltages for the microwave switch (LO multiplier switching) in the fundamental mixer are generated from this data word.

9.2.5 422 MHz IF switch (2) [2101-AQ1]

Various IF paths are switched through the "422 MHz IF switch" module depending on the input frequency of the spectrum analyzer (9 kHz to 3.2 GHz, Band 0; 3.1 to 26.5 GHz (30 GHz), Band 1 to 3; external 422 MHz input) (see circuit diagrams and block diagram).
The input signals for the IF switch are the 422 MHz IF output signals from the "Integration Band 0" [2101-ZA] and "Fundamental mixer" [2101-ZC] microwave modules, together with a third input for directly inputting a signal of frequency 422 MHz.
The IF switch thus corresponds in function to a 3-way single-pole signal source switch. The output signal is fed to the "422/22 MHz converter" board via the 422 MHz interdigital bandpass filter.

The three input signals (Band 0; Band 1 to 3; external 422 MHz input) have different levels. The various signal paths therefore include amplifiers and attenuators to set the overall gain to give approximately the same output level, regardless of operating mode.

Control and power supply are from the input section controller (5) [2101-AR]. The lines "Band 0" and "external" control four CMOS switches in the IF switch, which in turn control current sources for PIN diode switches.
A third control line allows a digitally-controlled current to be fed into the modules connected to the "422 MHz external" input socket of the IF switch to allow e.g. the diode working point of an external mixer to be optimized.

9.2.6 422 MHz/22 MHz converter (6) [2101-X]

The 422 MHz/22 MHz converter converts the IF signal from 421.99 MHz to 21.99 MHz.
It contains the following components:

- 422 MHz bandpass filter
- 400 MHz carrier generator
- 422 MHz/22 MHz converter
- Power supply

422 MHz bandpass filter IF-1

The 422 MHz bandpass filter, IF-1, suppresses the image receive point of the 422 MHz/22 MHz converter and unwanted products from the previous conversion. At the same time, it provides the 10 MHz resolution bandwidth (RBW).
The 422 MHz bandpass filter is an interdigital filter with capacitive truncated resonator.

400 MHz carrier generator

The 400 MHz carrier generator supplies the 400 MHz carrier for the 422 MHz/22 MHz converter. The carrier generator consists of a VCO, a switchable frequency divider and a phase-locked loop.

VCO

The VCO consists of active elements T 10 and T 11. A strip circuit serves as resonator; this is electrically expanded by the series circuit comprising C 66 and the varicap diodes GL 3 through GL 5. The signal is coupled out to the mixer via T 8 and T 9 and further to the frequency divider via T 5.

Frequency divider

The frequency divider divides the VCO frequency by 40 or 40.2. It comprises IC4.2, IC6 and the switchable 40/41:1 divider IC7.

Phase-locked loop

The PLL locks the VCO frequency to a 20 MHz reference frequency. It consists of a phase meter and a control amplifier. The phase meter IC3, IC4.1 compares the divided VCO frequency with the 20 MHz reference frequency divided by 2.
The output signals of the phase meter are each integrated by a RC low-pass filter and fed to a control amplifier, IC5. This sets the working point for the VCO varicap diodes.

422 MHz/22 MHz converter

The 422 MHz/22 MHz converter converts the IF Signal from 421.99 MHz to 21.99 MHz. It comprises input amplifier IC13, ring mixer IC9, and 22 MHz amplifier IC8, each of which is decoupled from the other by attenuators, and carrier amplifier T 12. Amplifier IC15 is for adjusting the input section gain and compensates for the thermal drift of the input section.

Power supply

The power supply provides +10.5 V, -10 V and +5.2 V for the circuit.

9.3 IF measurement section (7), (8), (9), (10), (11)

The IF measurement section contains the following modules:

- IF selection (7) [2101-L], [2101-R], [2101-S]
- Logarithmizer (8) [2101-M], [2101-Q]
- IF converter (9) [2101-O]
- Calibration generator (11) [2101-N]
- measurement section controller (10) [2101-P]

The IF measurement section evaluates the input signal after conversion to the last IF (21.99 MHz).

IF selection and logarithmizer board

Firstly, the signal is filtered to the required resolution bandwidth and the input level is matched to the logarithmizer and AD converter section (IF filter and IF amplifier on the IF selection board). The signal is then logarithmized. The rectifier is integrated into the logarithmizer, i.e. an AC voltage is present at the input to the logarithmizer and the video signal, which is a DC voltage proportional to the logarithm of the input amplitude, is present at the output.

The logarithmizer also has an AC output (with virtually constant amplitude) which is required for the FM and search demodulators.

Calibration generator board

The FM demodulator can demodulate a frequency modulated input signal and output this as an audio signal to loudspeaker or headphones. The search demodulator can be used to audibly detect signals which are swamped by noise.

When AM signals are present, the video signal is the demodulated signal; this can be switched directly to the loudspeaker or headphones. The demodulators are on the calibration generator board.
A further function of the calibration generator is to generate the internal and external calibration levels. The calibration generator is a synthesizer, tunable from 17 to 27 MHz, having an extremely accurate output level over the entire frequency range. The signal can be switched to the IF selection input for calibration purposes. It is also available from a socket on the front panel to permit external calibration.
The calibration generator board also includes the power supply connection for the entire IF measurement section module.

IF converter board

The video signal now passes through a low-pass filter, the limit frequency of which is variable; this is the video filter. This has the task of attenuating the rectifier ripple and, where required, averaging the display (e.g. for noise signals).

An r.m.s. value generator can be connected in front of the video filter, to produce the real r.m.s. value of a mixed signal. After the video filter follow the two ADCs, one a fast 8-bit converter with a sampling rate of 20 MHz (a 10-bit converter is used from series C onwards) and one slow 16-bit converter running at 40 kHz. They convert in parallel. The 8-bit converter handles fast events, such as pulse measurements or measurements using fast sweep times in zero span mode. The slow, high-resolution converter is for the 'normal' measurements.

Measurement section controller board

The selection from the mass of converted values and their compression into a measurement value is the job of gate array 1. It supports the DSP in the further processing of the data.

Gate array 2 contains a 32-bit frequency counter, to which various signal sources can be connected. For example, the IF can be precisely counted and the input frequency exactly determined. Gate array 2 also contains the trigger generator. This allows complex trigger conditions to be set and processed for zero span operation.

The measurement section controller board also includes the address logic and the clock conditioning for the entire module.

A further part of the IF measurement section is the calibration generator. This is a synthesizer, tunable from 17 to 27 MHz, having an extremely accurate output level over the entire frequency range. The signal can be switched to the IF selection input for calibration purposes. It is also available from a socket on the front panel to permit external calibration (calibration generator board).

The calibration generator board also includes the power supply connection for the entire IF measurement section module.

9.3.1 IF selection (7) [2101-L]

Bu1 carries the measurement signal, Bu2 the calibration signal (internal calibration, -30 dBm). The switching between the two signals is by means of relay Rel1. The unused signal path is shorted to ground through diodes Gl2 or Gl3. For high measurement signal levels, (>-10 dBm) there is a 14 dB attenuator, comprising R43, R44, R45 and R52. This is switched in by relay Rel2.
The 3rd order high-pass filter comprising C14, C23 and L6, shapes the 10 MHz bandwidth of the bypass path and prevents overdriving the preamplifier stages with 7 MHz signal components.
After the high-pass filter, there is a 12 dB wideband amplifier (Z_0 = 50 Ω). This consists of T2 and UE1, the gain being determined by the transformer ratio of UE1. After this, amplifier stage V1 amplifies the signal by a quasi-continuous (256 bit) factor of 0 to +6 dB. The gain depends on the control current through the PIN diodes Gl4 [2101-L] and Gl61 [2101-S], and the size of the control current depends on the data word at the input of DAC IC11. If link Br17.1-18 is closed, the maximum gain of V1 = V_{max} = 6 dB (approx.), if link 17 is removed, the gain is V = 0 dB. In measurement mode, Br17.1-17.2 is closed.
The signal can be passed into one of the three possible paths with the aid of the multiplexer IC1.1, IC2, IC6 or IC7.

- Bypass path, with a bandwidth of more than 10 MHz
- LC filter path, bandwidths 3 MHz to 100 kHz
- Crystal filter path, bandwidths 30 kHz to 1 kHz.

The signal collected by IC2 is passed to the input of the first (V2) of four wideband amplifiers (amplifier stages V2, V3, V4, V5).
The overall gain can be set in 1 dB steps in a range covering 61 dB.

The center-band frequency of the selection paths is 21.99 MHz.

The quasi-continuous (255 bit) alteration of the bandwidths is achieved with the aid of PIN diodes which have the function of a controllable damping resistor for the LC or crystal filter circuits. The control current through the PIN diodes is derived from the data word at the input of the DAC IC12.

S1 is only operated for adjusting the LC bandpass filters or for troubleshooting. The operational position is all switches set to "off".

The band center frequency of the LC circuits is pulled back to F = 21.99 MHz if drift occurs within about ± 100 kHz. Varicap diodes (GI82) on the LC bandpass filter board [2101-R] are used for this. The pulling voltage is generated in the DAC IC12 and can be checked at wire link BR15.1.

The thermal variation in the insertion loss of the LC circuits is compensated approximately by making the degree of positive feedback temperature dependent using R97 (NTC).

The signal selected by IC7 is fed to the output amplifier (IC19). The gain is +12 dB.

At the output of IC19 the signal branches to Bu3, TP14 and to Bu4 or Bu10 [60] (IF output) on the instrument back panel via T 303.

The input of the logarithmizers is connected to Bu3. The nominal level (calibration) at this point is +12 dBm or +3 dB or 1.5 V_{pk}. A voltage divider with a = 23 dB and Ri = 50 Ω is connected to the output of T303, so that the nominal level (calibration) at Bu4 is -20 dB.

Level detectors are directly connected to the input and output of the IF selection (T3,4,5 and GL6 with TP2 or GL300). Detection of the presence of the calibration level takes place in the comparator pair IC10. If the calibration level is present, TP20 or TP21 are "LOW".

GL103 is a 6.4 V voltage reference element. IC5 and T102 generate a working point of approx. -7.8 V referred to the +5 V supply voltage for the multiplexer IC3 and IC4. This voltage can also be measured at TP10. This ensures that the gain of the amplifier stages V2, V3, V4 and V5 is independent of variations in the +5 V supply voltage. To compensate for the thermal effects, NTC resistor R136 is inserted in the feedback path to IC5.1.
A -10 V reference voltage is present at TP15. This is generated by inversion of +10 V at GL400 by IC9.1 and T401 (reference voltage for DAC IC12). All current sources (gain V1, bandwidths in LC and crystal paths) are referred to this reference voltage.

Link BR15 is closed for normal operation. For adjusting the LC bandpass filters, an average control voltage of +5 V can be fed to the varicap diodes GI82 [2101-R] by closing the link BR15.2-16.

The LC circuits can be trimmed by ± 100 kHz (at least ± 75 kHz) with control voltages in the range +(2.5 to 10 V) and thus held to the band center frequency (21.99 MHz) to compensate for thermal drift or aging.

The addresses IF A1, IF A2, IF A3, IF A4, BGS IF SEL, the control data IF D0 to IF D7 and the +12 V, -12 V supply voltages are fed, preselected, from the "measurement section controller" board and are fed onto the "IF selection" board [2101-L] via plug St1.

HIGH level at BGS IF SEL activates the IF selection board for accepting addresses and data. The addresses are used to select operations, e.g. "fine level setting", "select filter type", "IF gain", "DAC register" and "update". The data (IF D0 to IF D7) indicate the value to be set.

9.3.2 Logarithmizer (8) [2101-M]

The simplified block diagram (see figure 9-4 on page 9-15) shows the interworking of the various function blocks. The logarithmizer basically consists of a chain of 10 amplifier stages, each with 10 dB gain, with a rectifier connected to each of their outputs. The rectifiers must all have the same characteristic which must also have a defined lower threshold (i.e. a response threshold for low levels) and an upper saturation limit for large levels. The rectifier outputs supply a current to the input of the adder stage. The sum current is a direct measure of the logarithm of the level at the input of the amplifier chain. After passing through a video low-pass filter with an upper limit frequency of 10 MHz, the signal is amplified to the required level by the output amplifier. The output of this amplifier feeds the output sockets to the ADC and, via an RC high-pass filter on the calibration generator board, to the demodulator.

At the input of the logarithmizer, there is first a 10 MHz bandpass filter with a center frequency of 22 MHz. The filter function requires an input source impedance of 50 Ω. The filter is unbalanced in order to compensate for the rectifier frequency response. A balun is connected to the filter, followed by a 0 dB buffer amplifier/impedance converter. The first 10 dB amplifier and rectifier are connected to the output of this buffer amplifier.

The noise filter is connected between the sixth and seventh 10 dB amplifier stages. The bandwidth of this filter can be switched in up to 4 steps. The filter band limits the wideband noise which is generated and amplified by the preceding stages.
This prevents the last four amplifier or rectifier stages from being saturated by wideband noise when narrow resolution bandwidths are set in the selection section. The bandwidth of the noise filter must, however, be matched to the resolution bandwidth (see table 9-1). A calibration facility must also be used to ensure that the center frequency is exactly 21.99 MHz and that the insertion loss of the filter is 0 dB.

Noise bandwidth	Use for resolution bandwidth (RBW)
> 10 MHz (bypass path)	≥ 1 MHz
1 MHz	300 kHz
400 kHz	1 kHz to 100 kHz
170 kHz	not used in SNA

Table 9-1 Relationship between noise filter bandwidth setting and selected resolution bandwidth (RBW)

For linear rectification, one of the total of 11 rectifier stages can be selected (i.e. the other 10 are disabled). For linear rectification, the lower response threshold of the rectifier is reduced and the gain of the output amplifier increased.

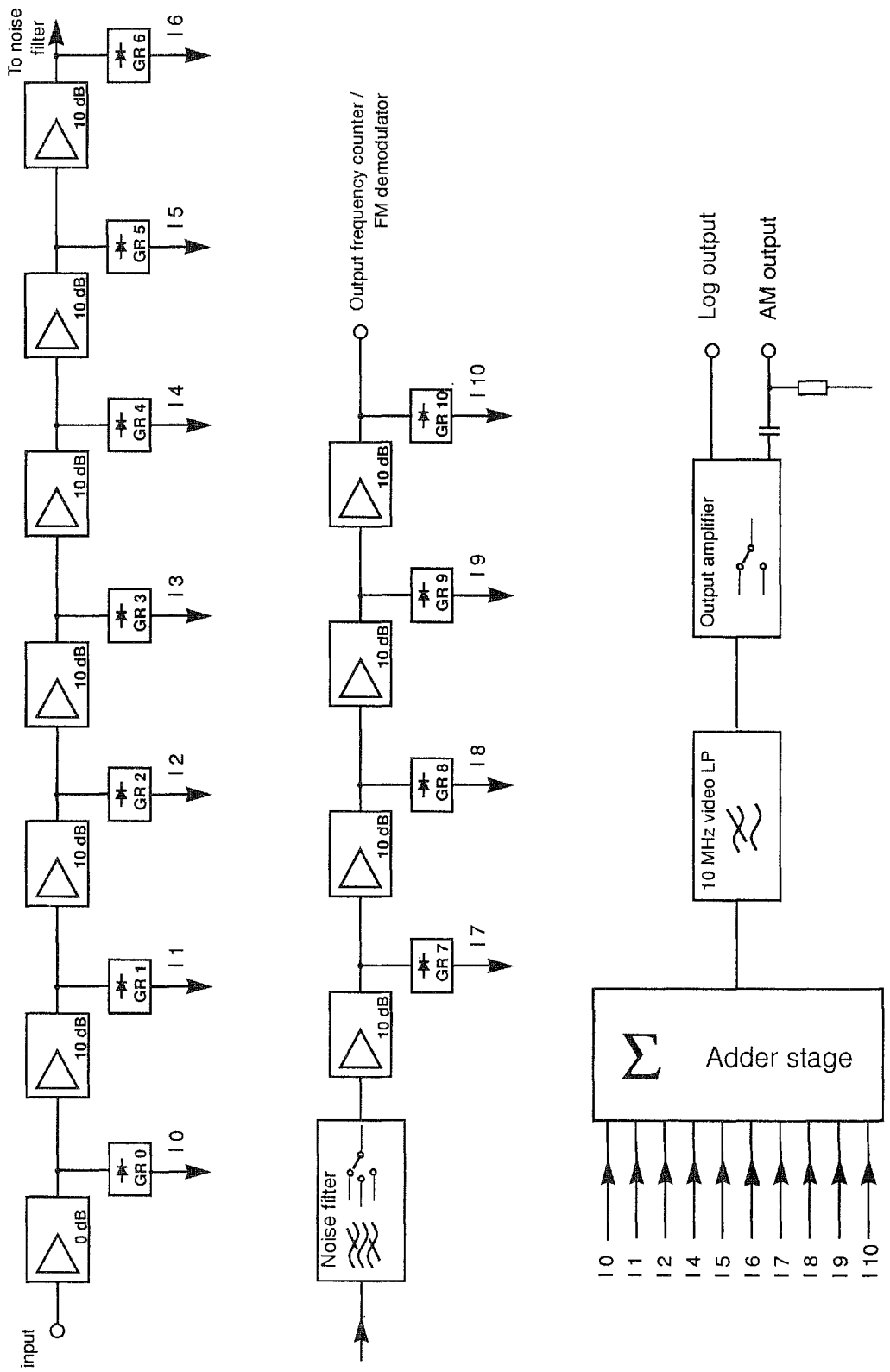


Fig. 9-4 Simplified block diagram of the logarithmizer (8)

The 10 dB log stages

The balanced layout of the 10 dB log stages (8) [2101-Q] is shown in the circuit diagram. The transistors T152 and T153 supply the gain and work in push-pull. They are coupled by the common emitter current source comprising T151 and emitter resistor R151. The coarse gain is determined by the ratio of the emitter resistors R155 and R156 to the collector resistors R158 and R161. P151 allows fine adjustment of the gain. R157 and C158 provide frequency response correction. Transistors T154 and T155 are connected as emitter follower and act as buffer stages for low-impedance drive of the rectifier and the subsequent amplifier stages.

The rectifier circuit is shown separately in figure 9-5 on page 9-16. L1, L2, R5 and R6 form two current sources together with the -10.9 V voltage source. In the idle state, their current flows through the diodes D1 and D2, via resistors R1und R2 and the balun to the rectifier voltage source (approx -5.1 V). If a signal of sufficient amplitude is supplied from the previous stage, the current is divided between the resistor pairs R1/R2 and R3/R4 with increasing amplitude. This leads to a signal current on the collective line (X). The maximum signal current (saturation state) is reached when half of the saturation current of each current source flows on the collective line. The bias voltage of the collective current line can be altered for linear rectification such that a small idle current flows on the line (switched on the main board [2101-M]). The field effect transistors for disabling the rectifiers are also located on the main board.

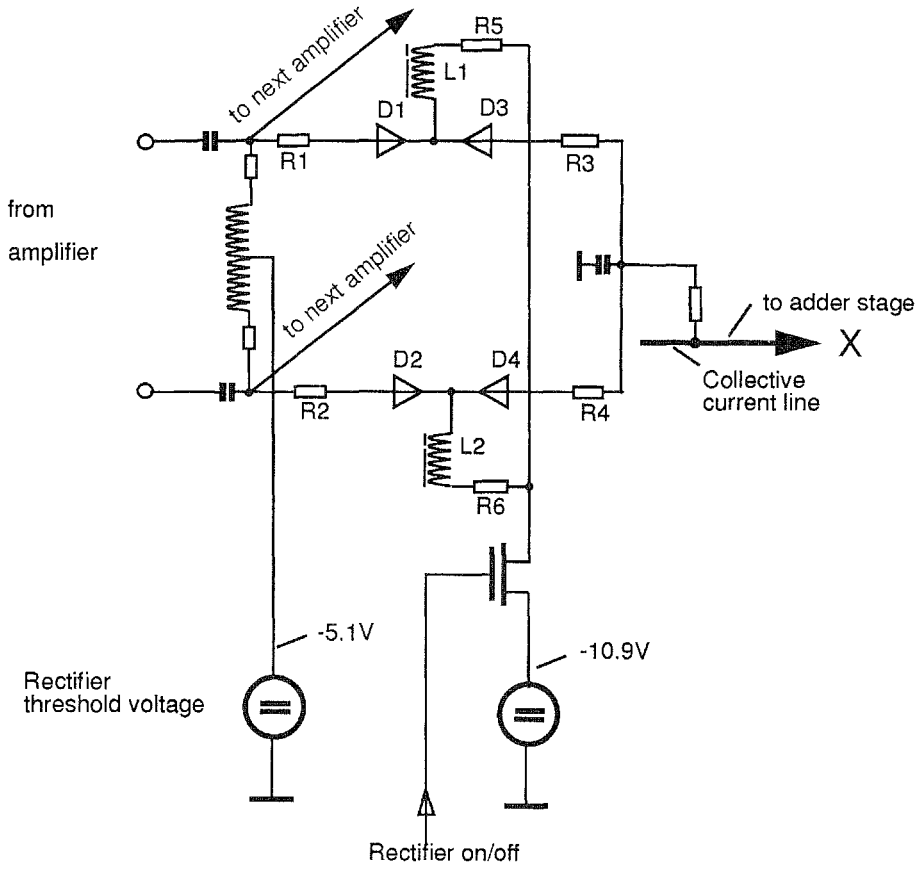


Fig. 9-5 Rectifier stage circuit diagram

The noise filter

The transistors T200 to T203 are connected as a balanced buffer with 0 dB gain. The outputs pass via two decoupling capacitors and a balun to the filter and a bypass path.
The bypass path serves for transmitting the wideband signals (1 to 10 MHz). The bypass path components form a bandpass filter with a bandwidth of >10 MHz. The signal is passed on to the buffer amplifier IC21 and IC22 via analog switch IC20 and on to the next log stage.
The actual filter comprises a deattenuated LC circuit, several resistors for fixing the bandwidths and several control elements. The LC circuit comprises L208, C215 to C218 and varicap diodes GL204 to GL207. The varicap diodes allow the center frequency to be set by a computer via a DAC.
The deattenuation is realized by analog switch IC20, buffer amplifiers IC21, IC22, diodes GL208/GL209 and R230/R231. The DC through the PIN diodes (GL208, GL209) can be varied using a DAC, so allowing the degree of positive feedback to be changed. In this way, the gain of the noise filter is set to 0 dB by the computer. The control current for the PIN diodes is fed in via resistors R227 and R228.
The narrowest bandwidth of about 400 kHz is set by R215 and R216. They are in series with the output impedance of the preceding buffer amplifier and damp the LC circuit. The PIN diodes GL200 to GL203 can be switched to low impedance via the control lines P (400 kHz NBW) and O (1 MHz NBW), the damping of the LC circuit being further increased through the resistors R213 and R218 or R218 and R219.
The analog switch selects between the bypass and the filter path via control line N (10 MHz NBW).

Adder circuit and video filter/amplifier

The rectifier currents are collected together on the collective current line (X) to form a sum signal. To eliminate feedback, the bias voltage on the collective line must be kept constant (Z = 0 Ω). This is achieved by the adder circuit.
The collective line is fed into the inverting input of the OP IC40.2. This is held to the same bias voltage as the non-inverting input by feedback (T400). When "Log scale" is selected, this voltage is about -6.0 V; for linear scale, it is approx. -5.5 V. The current is available from high impedance at the collector of T400, and is passed on to the finite input impedance of the 10 MHz video filter. To ensure the function for frequencies up to 10 MHz, T400 takes up the higher frequency signals in common base mode. The base impedance is reduced for this by C403 and R406. Additionally, an idle current is forced on the emitter of the transistor to ensure correct function of the circuit at low input signal levels. The double transistor T401 serves as current source for this. The second transistor generates an identical current which is subtracted from the signal current again via IC40.1 to restore the correct zero point. T402 and T403 (FET) switch the gain, the additional elements being required for gain-independent frequency response.

Threshold and bias voltage generators

All important voltages are based on the same reference, the Zener diode GL500. One rectifier threshold voltage (-5 VT) is derived directly from this reference via buffer stage IC51.2/T503. IC50.2 forms a current source with T502 and R514, P501 being used to set the current. This current produces a voltage drop across R516 and GL506 which is added to the reference voltage at the output of IC50.1. This voltage is used as the bias voltage via the adder for the collective current line in the "Logarithmic" setting. For the "Linear" setting, the bias voltage is switched to a value between the threshold voltage and the "Log" bias voltage using analog switch IC60.1. This intermediate voltage is set by P502. The -10.9 V for the rectifier current sources are generated in a similar way. They are based on the "Log" bias voltage. IC50.1 with T500 and R500 are used as current source. This current produces a voltage drop across R506 which is added to the above-mentioned bias voltage and the threshold voltages of diodes GL507 and GL508 which provide thermal compensation.

The working point setting (i.e. generation of the base voltages for the current source transistors in the 10 dB log stages) is referred to the -12 V supply. The base voltage is around 4 V higher than the -12 V supply.

9.3.3 IF converter (9) [2101-O]

The following functions are implemented on the IF converter board [2101-O]:

- Video filter
- 8-bit ADC (10-bit from series C)
- 16-bit ADC
- Multiplexers for gate time, frequency counter and trigger conditions for the 16-bit ADC
- RMS detector

Video filter

The first main part of the module is the video filter (resistors and capacitors between IC2 and IC7). These are simple RC lowpass filters, switchable in decade steps of in 3, 10, 30 from 3 Hz to 3 MHz. There is also a wideband path for the 10 MHz video bandwidth.
At the input of the video filter is a multiplexer (IC2) which switches the following signals to the video filter:

- the video signal; voltage range 0 to 5 V
- an external signal fed in to BU2 (y external)
  Voltage range: 0 to 1V (Gate of T304 HIGH)
  -0.5 to +0.5 V (Gate of T304 LOW)
- signal from r.m.s. rectifier; 0 to 5 V

The multiplexer IC7 together with the transistors T100 to T105 serves for selecting the video bandwidths.

8-bit and 16-bit ADCs

The signal is fed to the fast 8-bit ADC (IC16) via a buffer stage (IC13) and matching amplifier with subsequent driver (IC14 and T301). The output data from the ADC are fed via a latch (IC17) to the plug to the measurement section controller (ST1).
The same signal as is fed to the fast 8-bit ADC is also fed to the 16-bit ADC (IC20) via another matching amplifier (IC18). The data from this converter are read out serially and converted into a parallel 16-bit word by shift registers (IC21 and 22); this is also fed to the plug to the measurement section controller (ST1).
Latch IC24 is used to set the status word of the converter.
The reference voltages for the converters are derived from the reference voltage source IC11. IC12 and T300 generate -2 V for then 8-bit converter; IC19 generates +5 V for the 16-bit converter.
T304 (on IC11) can be used to insert an offset of half the screen area into the signal path. This allows a signal balanced about earth to be fed into the y external input.

Multiplexers for gate time, frequency counter and trigger conditions

The multiplexers for gate time, trigger and frequency counter functions (IC27, 28 and 29) are fitted on this board. The multiplexers are used to switch between the different input signals. IC25 is a comparator which triggers when the video signal exceeds a threshold which can be set via the DAC (IC26).

RMS detector

The rms detector is also on this board (IC8, 9, 10, 15 and 33)
The signal from the logarithmizer (video signal) is divided (R207-R210, R221), buffered (IC9) and antilogged by IC33.1. It is then averaged by R205 and C202 and fed via current mirror (IC8.1 with R203 and T202 with R204) to transistor IC33.4 where it is re-logarithmized. It is then coupled out via IC8.2 and amplified to correspond with the input attenuation.

9.3.4 Calibration generator (11)[2101-N]

Two completely separate function units are realized on the calibration generator board:

- Calibration synthesizer with level regulation
- Demodulators (FM, AM and search demodulator) with loudspeaker output stage

9.3.4.1 Calibration synthesizer with level regulation

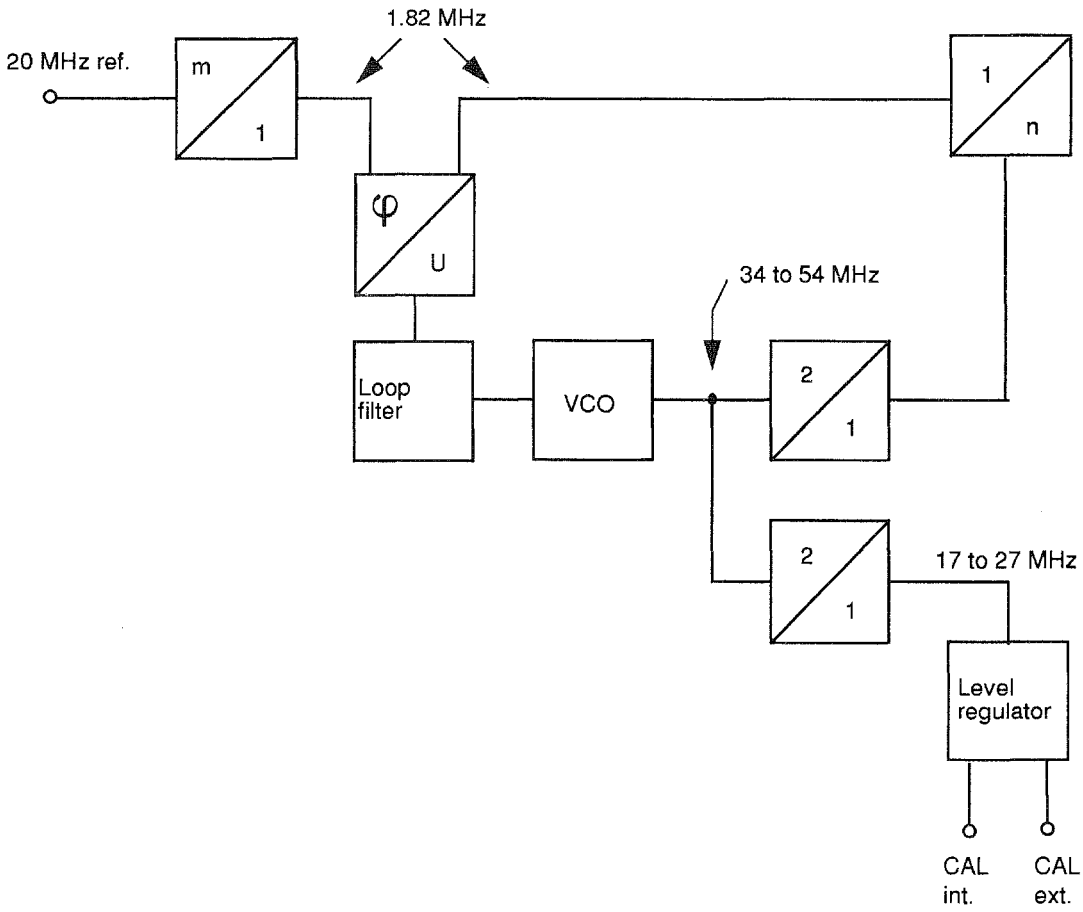


Fig. 9-6 Simplified block diagram of the calibration synthesizer

Synthesizer

The m/1 divider (IC6 and IC7) is normally set to m = 11 but can be set by software to other values.
The phase meter (IC2, IC3 and IC4) basically comprises an up/down counter (IC4) which counts back and forth between states 1 and 2 when locked. In the unlocked state, the counter either remains in state 0 (VCO frequency too high) or in state 3 (VCO frequency too low) until the control loop locks again.
The loop filter comprises IC1, R100-R109, C100-C108. The VCO comes next. It operates in the frequency range 34 to 54 MHz. It can be disabled via GL101.
IC10 forms the two 2/1 dividers. The n/1 divider is formed from the programmable divider PLLIA (IC8), together with IC9 for synchronization. The value of n for the PLLIA - and hence the output frequency - is set via the data lines IF D(0) to IF D(7) by the measurement section controller [2101-P]. The selection of the calibration generator module [2101-N] is via the address lines IF A1 to IF A4.
The IDBY(7:0) of the PLLIA are status bits which can be read by the main processor.

Level regulator

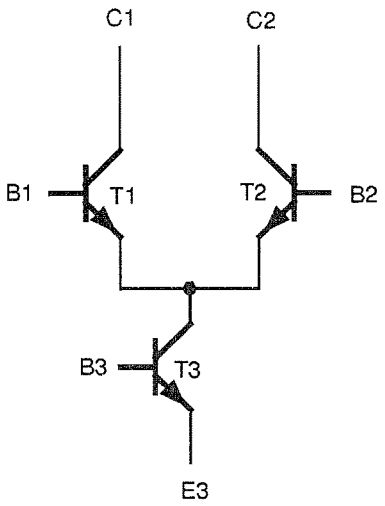


Fig. 9-7 Basic circuit, IC20.1, IC20.2

IC20 consists of two differential stages with current source transistors (see figure 9-7). The differential stages are connected as squarewave generators. Square waves with a duty cycle of exactly 1:1 are present at IC20.11 and 12. The current I in the second stage is controlled by keeping the voltage across R228 constant (IC21 forms an integrator with R242 and C213). The square wave drive causes T1 and T2 to pas the complete current I alternately. The output amplitudes at Bu2 and Bu3 are thus only dependent on the (controlled) current I and the collector resistances. Current I can be set with P2. P1 sets the level of the CAL EXT output separately.

9.3.4.2 Demodulators and output amplifier

FM demodulator

The FM demodulator is made up from IC31 and the resonant circuit formed by UE2 and C317/ C318. IC31 contains an active demodulator, on to one input (Pin1 and 4) of which the input signal (balanced by UE3) is passed. The other input (Pin8 and 10) is connected to the resonant circuit UE2 and C317/C318. This is coupled to the input signal via C319 and C320 and adjusted to the center frequency (21.99 MHz) by C317. For frequencies other than the center frequency, a phase offset is produced between the input signal and the resonant circuit which is proportional to the frequency difference; causing a change in DC voltage at the output (Pin 12).

Search demodulator

The search demodulator has the task of rendering audible weak signals which are practically swamped by noise. It comprises IC30, the demodulator, and Q1 with C300, C302 and C303, the oscillator. The signal is input to one input of the demodulator (Pin8); the other (Pin1 and 4) is connected to the oscillator which runs at 21.99 MHz. The difference frequency appears at IC30.12. If the search demodulator is not selected, the oscillator is disabled via IC32.

AM demodulator

The video signal of the logarithmizer is the AM demodulated signal. It is output directly to the output amplifier via the multiplexer IC32.

Output amplifier

The headphone output has two identical channels (IC36.1 and 36.2) for stereo headphones. The volume is set via IC34. The loudspeaker output volume is also set via IC34.

The computer warning beep is output to the SNA loudspeaker via the beep circuit. Loud and soft can be selected with T300.

9.3.5 Measurement section controller (10) [2101-P]

The function of the measurement section controller is basically to process the analog levels measured by the IF measurement section digitally in such a way that they can be displayed on the screen by the graphics processor. Calculations such as frequency response and level correction are included in the function. This module also includes the complete trigger circuitry for the instrument and the facilities for frequency measurement.

In "Spectrum analysis" mode, the entire SWEEP is split into max. 4000 equidistant measurement intervals. The IF level values sampled by the two ADCs in one interval are processed by a gate array (IC44) so that the characteristic data such as MINIMUM, MAXIMUM, etc. for the measurement interval are made available to a digital signal processor (DSP). The collection of measurement values is controlled by the synthesizer via a port reserved for this purpose, so that the sampled values can be correctly assigned to their corresponding frequency settings. The signal processor (DSP) stores these (4000) pairs of values processed by the gate array in memory. After appropriate further processing, the measurement data are compressed to 500 pairs of values and read by the graphics processor via a port and displayed on the screen. The collection and storage of 4000 values has the advantage that the trace can be expanded (zoomed) by up to a factor of 8 after the measurement.
As well as the above-mentioned MINIMUM and MAXIMUM values, the gate array also provides the information required for realizing e.g. the "AVERAGE FUNCTION", which is also calculated by the DSP.
The measurement is started with a trigger signal which is generated by gate array 2 (IC46).

The array IC44 is configured and "operated" via the signal processor, which in turn is in direct communication with the main processor. In contrast, the trigger array IC46 is controlled directly by the AT CPU via an 8-bit wide data bus.
The trigger array gets the signal from the 8-bit ADC. Various conditions can be set via the main processor for generating and outputting a trigger signal. The further processing of this trigger signal depends on the operating mode and the instrument settings. This signal can be used to start a measurement or to synchronize an external test instrument as the trigger signal is also output to the ext. trigger connection.
As well as the trigger circuits, this gate array also contains a 32-bit wide frequency counter which can make frequency measurements with fixed gate times and period duration measurements over a selectable (limited range) of periods. It is also possible to control the gate time externally and subsequently calculate the frequency. The input signal of the frequency counter is digital, coming from a multiplexer on the IF converter board, so that the frequencies of various signal sources can be measured.

9.4 Synthesizer BN 2101 (OD-11)

The synthesizer OD-11 is used in several instruments. Not all of the features of this universal module are used for the SNA-20/-23. The following circuit description includes all possible features of the synthesizer. Those features not used in the SNA are marked accordingly.

9.4.1 Standard frequency oscillator, NFO adapter (50) [2101-C]

The standard frequency oscillator supplies a 10 MHz sinewave signal (ST101 or BU101 Pin 9 "10MHZRF") which is used as a reference by the synthesizer and from which it derives its frequency accuracy (long- and short-term stability). The short-term stability (phase noise) of the synthesizers for a control bandwidth of, say, 10 kHz is set by the standard frequency oscillator up to a frequency offset of 1 kHz. The standard frequency oscillator is a thermally stabilized crystal oscillator (OCXO). The absolute frequency can be set via potentiometer P101 or via the control input "UVCO" BU101.5 or ST101.5 (for external 10 MHz synchronization).

9.4.2 YIG oscillator OS1 (50), YTO

The YIG oscillator is a current-controlled oscillator for the frequency range 3.1 to 8 GHz which can be synchronized by the synthesizer to the standard frequency oscillator via a PLL (internal control) or operated as a voltage controlled oscillator. The YIG oscillator is controlled using two control coils: The tuning coil serves for setting the frequency and has a large control slope at high inductance; the FM coil has low control slope and inductance and is used for frequency modulation (rapid tuning). The frequency modulation function is not used by the SNA.

9.4.3 Timebase/YTO driver [2101-B]

9.4.3.1 Central filter (DC-PREFILTER)

The central filter serves as a pre-filter and suppresses interference voltages for the supply voltages from the AC PSU before they are fed to the individual modules of the synthesizer. The ± 6.5 V and ± 12 V supplies are filtered by a low-noise OP filter in each case and the +18 V supply by a passive filter. The function is described using the +12 V OP filter as an example. The OP filter +12 V compares the ground potential IC41 Pin 3 as nominal value with the AC coupled +11.8 V actual value at IC41 Pin 2. The resulting amplified correction voltage at IC41 Pin 6 is input in antiphase to the interference voltage. The filter circuits for -12 V and ± 6.5 V operate in the same way.

9.4.3.2 Timebase

The timebase circuit provides various frequency reference signals for internal and external modules. The circuit basically comprises the following function units:

- Timebase filter
- Timebase 1 (external synchronization control circuit)
- Timebase 2 (400 MHz PLL)

Timebase filter

The supply voltages from the central filter are filtered by this circuit again using low-noise active filters similar to those in the central filter (see section 9.4.3.1) to give the required suppression of AC interference voltages for the timebase reference signals. OP filters (IC8, 9) are used to derive +5 V and -5.2 V from the +6.3 V and -6.3 V rails and transistor filters (T2, T8 and T9) to derive ± 10.5 V from the ± 11.8 V rails.

Timebase 1 (external synchronization, 10 MHz)

A 10 MHz signal at the "Fext10Mz" input (BU1), after conversion to TTL level (IC1) and amplification (T1) is detected by a peak value detector (GL3, GL4,C4,C6 and R12) and closes a slow PLL via the control signal IC4.4 Pin 8 *(control bandwidth approx. 14 Hz)*. The standard frequency oscillator (OS101) is operated as a voltage controlled oscillator (control input "UVCO" ST101 or BU101 Pin 5). Its 10 MHz signal ("10MHZRF" ST101 or BU101 Pin 9) is fed to the comparator side of a FACT frequency/phase detector (IC31 and IC15.4) after conversion to FACT level by the limiter amplifier (T3) and is compared in phase and frequency with the external 10 MHz signal. The resulting control voltage pulls the frequency or phase of the standard frequency oscillator via PI controller (IC6.2) to achieve synchronization to the external 10 MHz signal.

A signal that the operating frequency accuracy of the standard frequency oscillator has been reached after a cold start is given by the "OVEN_WARM" status signal. This signal is derived from the current detected (via R14) drawn from the oven of the standard frequency oscillator.

Timebase 2 (400 MHz PLL)

The 400 MHz oscillator [2101-F] is locked to the standard frequency oscillator by a PLL. For this, the 400 MHz signal is passed through a frequency divider chain (10:1 Ecl divider IC3 and two 2:1 Fact dividers IC12) to divide it by 40 and fed to the comparator side of a FACT frequency/phase detector (IC32 and IC5.1) and is compared with the 10 MHz signal of the standard frequency oscillators ("10MHz" IC32.2 Pin 11). The resulting control voltage pulls the frequency or phase of the 400 MHz oscillator via PI controller (IC35) and locks the loop. As the 400 MHz PLL has a control bandwidth of 1 kHz, the short-term stability (phase noise) for offset frequencies above 1 kHz is determined by the free-running 400 MHz oscillator.

The following timebase output signals are provided from this module:

- 400 MHz sinewave, 0 dBm/50 Ω ("400MHZ" at BU7)
- three 20 MHz signals with Fact level ("20MHZ_1", BU3 to "20MHZ_3" BU5)
- an inverted 20 MHz pulse with a pulse width of approx. 4 nsec at ECL level ("PD_20MHz" at BU8)
- 10 MHz, 0 dBm/75 Ω ("10MHZ_RW" at BU2)

9.4.3.3 Controller/YTO driver

This circuit module includes the switchable control amplifier (PI controller) for the YTO PLL and the voltage/current converter for driving the YTO.

Controller/YTO driver 1 (PLL mode)

The differential output signal of the phase meter [2101-K] at (50) IC18 and TP 13) is first passed parallel to the controller signal path of the YTO PLL to a double-way rectifier with following Schmitt trigger (IC17) to generate the signal "YTO_SYNC". This status signal indicates synchronicity of the YTO PLL in fixed frequency operation (in CW mode, the phase meter output voltage is approx. 0 V in the locked state).
The phase meter correction voltage can be weighted with two separately switched filters (IC22 and C62 to C66, L33, L34) in the signal path. These serve to suppress the incremental frequency and its harmonics during a frequency sweep, switching being every 19.2 µs. The gain of the subsequent non-inverting amplifier (IC19) can be controlled via the "VLIN" circuit (compare Controller/YTO driver 2). After this, the gain and corner frequency required for a particular control bandwidth are set in the first part of the circuit (IC23). Four control bandwidths are available; these are set by the analog switch (IC25) which is programmed from the DSP (synthesizer controller). The control bandwidths are 100 Hz, 3 kHz, 10 kHz (default setting) and 30 kHz (rapid tuning). The "INTEGRATOR" control signal is fed to an integrating voltage-controlled current source (IC26 and T16) and drives the YIG TC coil in the case of internal control. A resistor in parallel with the YTO TC coil (R221) which serves to reduce the frequency dependent slope of the YTO TC coil (1st order low-pass filter) is switched out for the 30 kHz control bandwidth by a switchable inductor (L11).

Controller/YTO driver 2 (VLD mode)

When the YTO is controlled externally (this function is not required in the SNA), a relay (REL1) is used to switch to a parallel voltage-controlled current source (iC36 and T17). This allows the YTO to be controlled via the differential "VC/VC_N" input ST15 Pin 2 and 1.

In both cases, the current-proportional voltages across the measurement resistors of the YIG driver (R152 or R153) are tapped to generate frequency-proportional control signals. This signal (TP22) can be used to realize linearization of the control loop gain for the internal PLL. For this, the loop gain is incremented in two steps by reducing the resistance (R109) with the frequency via the signal line "VLIN" (compare Controller/YTO driver 1), to compensate for the frequency dividing factor which drops with the frequency.

A frequency span provided for an internal 18 Hz sinusoidal sweep can be switched on to the differential output signal "F_MON" via bandpass filter IC24 at connections HO24 and 25 for evaluation by the DSP. For externally controlled operation (signal tapped from TP23), a superimposed frequency span can also be switched on to the differential output signal "F_MON" via high-pass amplifier IC47 for measurement by the DSP (this function is not used in the SNA).

YTO frequency limiter

Regardless of the YIG driver which is used, a limiter circuit (IC38 and T10,T11) operates when the YTO frequency limits are exceeded. The YTO current is detected via a measuring resistor (R206) and compared with an upper (IC38.2 Pin 6) and a lower (IC38.3 Pin 10) limit value. Depending on the result, an additional current is fed in via T10 or the excess current drained via T11.
The low-noise active OP filters IC28, IC29 and T23, and IC40 and T22 on this circuit section are used to generate the reference voltages "+5 VREF", "-5 VYTO" and "+15 VYTO".

Serial interface to synthesizer controller

The programmable switches are set by the synthesizer controller DSP using the static control signals "DS(0)" to "DS(15)" via the serial interface to the synthesizer controller (IC45 and IC46 with the signals "DATA" ST9 Pin 24, "SHIFTCLK" ST9 Pin 23 and "LATCHCLK" ST9 Pin 22).

Synthesizer interface to frequency modulation

A synthesizer interface to frequency modulation is provided at BU17 by bringing out the connections to the YTO FM coil (not used in the SNA).

9.4.4 400 MHz oscillator ([2101-F]

The 400 MHz oscillator is a voltage controlled LC oscillator which is synchronized to the standard frequency oscillator by a PLL (compare Timebase 2).

9.4.5 Synchronous divider/phase meter (52), [2101-K]

9.4.5.1 Synchronous divider

In this part of the module, the YTO signal predivided by a factor of 16 in the SHF predivider module ("FYTO/16" at (52) BU20) is passed to a further frequency divider. This is a fractional divider which allows non-integer fractions of the 20 MHz reference frequency of the YTO PLL. This consists of an integer ECL frequency divider (IC2), the programming inputs of which are time-weighted with the aid of a computing algorithm realized in the gate array PLLIA (IC1). This produces frequency division which is fractional when averaged. The fractional division factor is written to the gate array (IC1) via the DSP (the synthesizer controller) from where it is passed to the ECL divider in the form of a specific sequence of whole-number program values.

Before the divided YTO signal ("ST_20MHZ" and "ST_20MHZ_N") reaches the comparator side of the frequency/phase detectors, it is resynchronized by passing through the D flip-flop IC6 (edge jitter limiting) and several gates (IC4 and IC5) which function as buffer stages for the ECL signal peaks. The output signal of the fractional divider is also used as the processor clock for the PLLIA gate array after conversion from ECL to HCMOS level and pulse widening (IC7 and T1 to T3).

In externally controlled YTO mode, the output signal of the fractional divider can be switched on to output "FYTO/400" (52) BU21 (T4 to T7). This output is used e.g. for YTO frequency measurement under external control. When the fractional divider is set to a fixed factor of 25, the overall factor with the predivider factor of 16 is 400 for the YTO signal.

9.4.5.2 Phase meter

The digital frequency/phase detector IC58 compares the 20 MHz reference signal "PD_20MHz" from the timebase at (52) BU40 with the divided YTO signal "ST_20MHz" or "ST_20MHzN" and thus generates a correction signal which re-locks a free running YTO by means of two-point regulation (frequency-sensitive range, synchronization to standard frequency oscillator) and which holds the YTO in a PLL if the YTO is locked (phase sensitive range, specific control bandwidth, e.g. 10 kHz). Gates (IC53 and IC54) are used to decouple the 20 MHz reference signal as in the synchronous divider. The correction signal must also be filtered by a 3rd order lowpass filter to remove the switching interference generated by the computing algorithm in the PLLIA gate array and to suppress the 20 MHz reference frequency.

9.4.6 Synthesizer controller (51), [2101-A]

The ADC interface (ADC PORT) consists of an ADC IC31 with preceding digitally programmable amplifiers (IC35, IC21 and IC36). A signal at the differential analog input "F_MON" ST12 Pin 2 and 1 can thus be sampled at intervals corresponding to the interrupt period of 19.2 µs (signal line "NIRQA") and read in by the DSP using digitally set scaling from DAC IC35.
In the INTERRUPT GENERATION circuit, the interrupt periods are generated by frequency division (IC33, IC34, IC32 and IC10.2) of the signal "CLK_10MHz". The signal "CLK_10MHz" is itself derived by division (IC17.1) of the DSP 20 MHz clock. The interrupt period "PINT" (19.2 µs) is programmable from the DSP. The "INTB" (3.35 s) interrupt period is fixed.
The address decoding for the I/O ports of the DSP (DSP-BUS ADDRESS DECODER) is realized using IC24, IC25, IC27, IC28, IC10.1 and IC10.4. The following components are selected via chip-select lines:

- Gate array PLLIA (compare "Synchronous divider" (52)IC1) via "CS1N"
- ADC IC31 via "CSADWN"
- DAC IC35 via "CSDACN".

The ports, which are passed via a flip-flop, receive a clock pulse when selected which switches the input data for the relevant port through to the port outputs:

- IC19 is activated via "SIC19CLK"
- IC18 is activated via "SIC18CLK"
- IC30 is activated via "SIC30CLK".

The serial output interface for setting the programmable switches on the timebase/YTO driver board and for "PINT" interrupt programming (IC19) are brought out to ports. The input interface for querying the status signals from the timebase/YTO driver board is also present (IC18). The interfaces (IC18 and IC30) are for various trigger input and output signals and for storing or reading synthesizer-specific information to/from the EEPROM (IC7).
The synthesizer controller has two 16-bit output ports. The first is the YTF port (IC2 and IC3) with its attendant data valid signal (YTFSTROBE) IC9.1. The X-ADDRESS PORT is formed by IC4 and IC5 and IC9.2 (XW_STROBE), and is the interface to the measurement section controller.
The PLLIA BUS (IC29, DSP data bus) for controlling the gate array PLLIA (52) IC1 is another interface.
The DSP-RAM module (IC6) expands the RAM available in the DSP.
Coupling of the DSP to the AT processor is realized via the DSP address decoder (IC15 and IC14), the read/write switch (IC22, IC17.2, IC10.3, IC13.1 to IC13.3) and the data bus direction switch (IC37).
The DSP can be set to RESET mode with the aid of the DSP control register (IC11 and IC16). The DSP clock can be generated asynchronously using the 20 MHz crystal (Q1) or synchronous to the timebase via the 20 MHz timebase signal "20MHZ_1" BU11.
The SYNC.PORT interface which can be used to synchronize two synthesizers, is not used in the SNA. The "PINT" interrupt circuit the period of which (19.2 µs) is used to increment the frequency during frequency sweeps can be looped from master to slave to achieve interrupt synchronization. Master/Slave switching is via the DSP control register, i.e. via the AT processor.

Controller filters

Active OP filters are used to filter the supply voltages. These operate in addition to those on the central filter board. The filters for the synchronous divider/phase meter (IC201,IC202, IC203) and the SHF predivider module (IC20) are also present in this circuit diagram.

9.4.7 SHF pre-divider module (53) [2101-ZG]

The YTO signal "FYTO" is (a) directly looped through the SHF predivider module to give the synthesizer RF output "1.LO", and (b) coupled in to a microwave amplifier (U3). This amplifier serves to isolate the subsequent microwave frequency predivider U2 from the YTO, as the divided frequency ("FYTO":8) and its harmonics are present as crosstalk on the divider input and would therefore appear at the YTO output if not decoupled. The YTO signal, predivided by 8 is then divided further by a factor of 2 in another frequency divider U1 to give the division factor 16. This signal ("FYTO/16") is then fed to the synchronous divider.

9.5 Controller (16), (17), (18), (19), (20), (21), (92)

The controller of the SNA-20/-23 contains the following modules:

- AT CPU (18)
- Memory (17) [2101-AF]
- Interface board (16) [2101-AG]
- Display control board (92) [4111-A]
- Keyboard (20) [2101-AJ]
- Rotary control (21) [2101 AK]
- Keyboard controller (19) [2101-AL]

9.5.1 AT CPU (18)[] series A through E (3011.9305.006)

The STANDARD SYSTEM MODULE 386-WGR is used as CPU in this instrument. This is an AT CPU with 80386SX/25 MHz processor, 4 MB RAM (expandable to 8MB) and 32 KB CACHE RAM. The circuit board is fitted with an EEPROM for storing and reading out instrument-specific data. This compact CPU board provides the following interfaces:

- AT bus interface with all address, data and control lines at P1 and P2
- Two serial interfaces (SERIAL PORT 1 and 2) at J1, J4 (port 2 is not fitted)
- One parallel interface at J5
- Interface for floppy disk (HD format, 1.44 MB)

9.5.2 Memory (17) [2101-AF] (series A through E only)

The memory board occupies the address range 580000hex to 5FFFFFhex and 920000hex to FBFFFFhex. It is connected electrically to the AT CPU (SIM386-WGR) via the 96-way and 48-way three-row strip connectors (J1, J2; CONTROL-BUS). All circuits on the 96-way and 48-way strip connectors are taken directly to the three 50-way ribbon cable connectors (P1, P2, P3) which also feed all of the CONTROL BUS lines to the interface board.

Power supply

The memory board requires the following supply voltages:

- 5V ± 5%; I = 400 mA
- 12V ± 5%; I = 60 mA

The supply voltages are fed from the interface board via the three 50-way ribbon cables. TTL levels are present on the signal circuits to the AT CPU and to the interface board. Memory board accesses are all 16-bit and are in the CPU memory area. The following timing is used: The bus clock is 8 MHz; one command delay and two wait states are inserted per cycle.

Decoding (see block circuit diagram)

The decoding is realized using seven PALs (U202 to U208). A "chip select" (NCSxy) signal is generated for each memory component. The address range for which the chip select is active is determined from the addresses and the signals ZWEIMB and NCSE. The NCSE signal is active-low and enables the chips selects when no RESET is present and memory access is required.
The memory control has EVEN and ODD or low byte and high byte structure, due to the 8-bit chip organization. If SA0 is LOW, the low byte is activated; if SBHE is LOW, the high byte is

activated. For 16-bit access, A0 and SBHE are LOW within one cycle.
Since SA0 is used to distinguish between EVEN and ODD, the lowest address for the memories is SA1.

Important: "Low byte components" have even chip select numbers (EVEN addresses).
"High byte components" have odd chip select numbers (ODD addresses).

RAM: (U300 to U304)

The SRAM capacity is 512 KB; it is battery-buffered (V_{batt} > 2.0 V). The chip organization is 128K x 8. The switch from +5 V to V_{batt} and vice-versa when switching the instrument on or off is realized using U306.
The lithium battery (BT1) which buffers the SRAMs is fitted on the memory board. It is plugged in for easy replacement. The SRAM contents may be partially or completely lost when the battery is replaced. The battery capacity is (depending on type) 1000 mAh or 750 mAh. The memory status port (U201.1) indicates whether the battery voltage is sufficient (V_{batt} >2.2 V) or too low to retain the SRAM contents (V_{batt} <2.2 V) (see memory status port).

Correction value memory (U512, U513)

This memory area is reserved for correction tables (e.g. frequency response corrections). This area is not used at present in the SNA, as the correction tables are stored in the battery buffered RAM.

These FLASH-EPROMs can be organized as 128 K x 8 (standard) or 256 K x 8 modules. The memory size must be the same as that of U400 to U413 and U500 to U511.
Jumper P210 must be set to match the memory modules used.

P210:
Pin 2,3 ON: 1 Mbit chips
Pin 1,2 ON: 2 Mbit chips. ON = Jumper fitted

To set the program voltage (+12 V ± 5%), the address 920000hex must be set. The program voltage is present until the address 920200hex is set. Decoding of this address range is by means of the PAL U204 (SVPP). The +12 V is switched to VPROG via Q701. VPROG is +5 V in read mode for the FLASH EPROMs.

Program memory (U400 to U413 and U500 to U511)

The SNA instrument software is stored in this memory area. The memory can be configured in four ways, depending on the settings of jumpers P210 and P211. The components must be fitted in pairs, because control is via low byte and high byte. The memory must be the same size as that of U512 and U513 (correction value memory).

Possible configurations:

P210 controls the input "ZWEIMB" of the decoder PALs.
Pin 2,3 ON; ZWEIMB = Low ==> 1 Mbit chips
Pin 2,1 ON: ZWEIMB = High ==> 2 Mbit chips

P211 sets whether EPROMs or FLASHs (U400 to U413 and U500 to U511) are fitted. The link setting feeds either "+5 V" or "VPROG" to the Vpp pin of the components.
Pin 2,3 ON; Vpp = +5 V ==> EPROMs fitted
Pin 2,1 ON: Vpp = VPROG ==> FLASHs fitted

Extended BIOS(U400...U401)

The extended BIOS is 64 kB and is part of the program memory.

Memory status port (U201.1)

The memory status port can be addressed in the range 921800hex to 9218FFhex. It is a 4-bit read port which provides the following information signals:

Data circuit D0

D0 is driven by the signal line "ZWEIMB".

HIGH	2 Mbit chips fitted	(U400 to U413 and U500 to U513)
LOW	1 Mbit chips fitted	(U400 to U413 and U500 to U513)

Data circuit D1

D1is driven by the signal line "NLOW_BAT".

HIGH	VBatt > 2.2 V	Battery o.k.
LOW	VBatt < 2.2 V	Battery requires immediate replacement.

Data circuit D2

D2 is driven by the signal line "HOT", which is fed to the memory board from the AC PSU via the interface board.

HIGH	Instrument temperature > Max. allowed component temperature ==> too hot
LOW	Instrument temperature < Max. allowed component temperature ==> o.k.

Data circuit D3

D3 is driven by the signal line "FLASH".

HIGH	FLASHs fitted	(U400 to U413 and U500 to U511)
LOW	EPROMs fitted	(U400 to U413 and U500 to U511)

Test points

MP200	NID-CS3	Chip select for the ID-EEPROM U200, active-low.
MP201	ID-SK	Clock for the ID-EEPROM U200.
MP202	ID-DATA	Data circuit for the ID-EEPROM U200.
MP203	NMEMCS16	Active-low output to CPU for enabling 16-bit access. NMEMCS16 is high-impedance outside the memory board address range.
MP204	MEMORY _STATUS	Chip select for the memory status port, active-low.
MP308	VCC1	Instrument on: VCC1 = 5 V Instrument off: 3,7 V>VCC1> 2,1 V.
MP309	NLOW_BAT	LOW if battery voltage is 2.2 V; otherwise HIGH.
MP700	SVPP	HIGH: Program voltage for the FLASHs = on. VPROG = +12 V. LOW: Program voltage for the FLASHs = off. VPROG = +5 V.

9.5.3 Interface board (16) [2101-AG]

The interface board is connected to the AT CPU, the memory board and the display control board via the CONTROL BUS. The CONTROL BUS signals are fed in via three 50-way ribbon cables via connectors ST1,ST2 and ST3 from the memory board (17) [2101-AF].The CONTROL BUS signals are fed from the interface board to the display control board via sockets BU1 and BU2.
The supply voltages from the voltage distribution board (1) [2101-BD] are fed to the interface board via ST16. The AT CPU, memory and display control boards are supplied with the supply voltages from the interface board (via the corresponding CONTROL BUS connections). Apart from distribution of the supply voltages and transfer of the CONTROL BUS, the following functions are found on the interface board:

- Chip select generation/control logic
- Timer
- IEC bus interface
- Interrupt controller
- Bus brake
- DMA bus interface
- Bus driver
- ID-EEPROM

Chip select generation/control logic

The various chip select signals are generated by IC10, IC11, IC13, IC14 (PAL), e.g. for IC12 (Interrupt Controller), IC15 (IEC bus), IC28 (Timer), IC21 (Bus brake) etc.Various control signals required on the interface board are also generated from logical combinations of CONTROL BUS signals and other control signals.

Timer

The timer is realized with time module IC28. The clock signals required for this module are derived by multiple division (IC9.2, IC26, IC27) from the 8 MHz CONTROL BUS clock. The timer generates the interrupt requests INT_TIMER0, INT_TIMER1 and INT_TIMER2 for the interrupt controller IC12.

IEC bus interface

The IEC bus interface is formed by the GPIB controller TMS9914 (IC15) and the bus drivers IC16 and IC17. The IEC bus of the SNA can be operated as a system controller.

Interrupt controller

A 92C59 (IC12) is used as interrupt controller. It generates the interrupt signal IEC_INT which is fed as IRQ10 to the CONTROL BUS from bus driver IC5.2 and which accesses the AT CPU for interrupt processing.

Bus brake

The bus brake circuit links the CONTROL BUS to the PERIPHERAL BUS. The circuit is formed by IC23, IC24 and IC33 (8-bit D latch) for the address bus and by IC22, IC25 (bus transceiver with register; bus transceiver) for the bidirectional data bus. The clock signals required for driving the components are generated by OS1, IC29.2 and IC21. The bus brake circuit is designed to minimize interference in the analog measurement sections caused by continual level changes on the address and data lines. The levels on these circuits are kept constant until renewed access to the peripheral bus is necessary.

DMA bus interface

IC30, IC31 and IC29.1 form a DMA interface. This allows the measurement section controller DSP (10) to directly access (DMA) the memory areas connected to the CONTROL BUS.

Bus drivers

The address, data and control lines of the CONTROL BUS are driven by bus drivers (IC1), (IC2), (IC3), (IC4), (IC5), (IC6), (IC19) and (IC32).

ID-EEPROM

Specific information about the interface board can be stored in or read from the ID-EEPROM (e.g. hardware status). The SNA's serial number is also stored in this EEPROM.

9.5.4 Display control board (92) [4111-A] (series A through E only)

The display control board (BSK-3) contains a VGA controller from Chips & Technology which is operated in EGA mode, and a graphic processor from TI, the TMS 34010. These two controllers make it possible to drive an EL display from FINLUX and an EGA monitor with TTL interface. Switching between the controllers and displays is via software (Instrument software menu: Mode, Configuration, Display, Display Screen INT/EXT).

The AT bus (CONTROL BUS) is fed to the BSK-3 via the 96-way and 48-way three-row connectors (P1, P2). The addresses (SA(19:0)) and various control signals are decoupled from the AT bus via bus drivers U38, U40, U5 and U39. The VGA chip requires a multiplexed address and data bus (IB). This is formed by bus drivers U35 and U37 for the addresses and U10 and U11 for the data. The VGA BIOS EPROM U71 is also connected to the internal 'IB' bus.

The VGA controller (82C455) is driven with a clock frequency of 32 MHz, with a pixel clock of 25 MHz for the CRT monitor (external monitor) and 16 MHz for the EL display. The VGA chip has 1 MB of video RAM (U12, U56 to U62).

For switching the TI processor (U63), the I/O decoding of the AT bus (CONTROL BUS) is needed. U31 (PAL22V10) decodes the higher value address lines for U4 (EP 910 -30), as well as MEMCS16 for the AT bus. U4 generates all the control signals required for the AT bus drivers and the host interface of the TI processor.

The TI processor can access local memory. This consists of 512 kB DRAM (U25 to U27) as TI processor program memory and 512 kB VRAM (U13 to U16) as video memory. A further 4 EPROMs (U17, U18, U21,U24) can be fitted as program memory for the TI processor (not used in the SNA).

The local memory access bus of the TI processor is a multiplexed address and data bus (TB_LAD(15:0)). The circuit for controlling the local memory of the TI processor is formed by the address multiplexer (U29, U23) for the addresses LB_MA(8:0) and the address latches U9 and U22 (LB_A(29:9)) for the EPROMs (U17, U18, U21,U24). The data lines for the memory bus (LB_D (15:0)) are generated by the bus drivers U19 and U53 from the multiplexed address and data bus (TB_LAD). U54 (PAL 22V10) decodes the addresses for the TI chip. The "CAS-before-RAS" refresh cycle logic is implemented with U30 and U6.

The TI processor has a 16-bit pixel bus (TS) with 4 bits per pixel. Each word therefore contains 4 pixels. This in turn requires 4 to 1 pixel multiplexing. U32 and U36 form the first 2:1 multiplexer and U51 (PAL) forms the second. U51 also switches the pixel clock for the TI processor. Clock signal blanking for the serial VRAMs (U13 to U16) is done with U47, U6 and counter U90.

U8 forms the EL interface register and U20 is the CRT interface register for selecting the mapping EPROMs U44, U43 and blanking the CRT monitor. U41 latches the data pixels of the VGA chip. The individual pixels from the TI and VGA controllers are stored in U42 and U45 to provide synchronization with the clock signals and stable addresses for the color table EPROMs U43 and U44.

Up to 16 mapping tables can be stored for each controller in the CRT EPROM U44. The selection of individual bits is via multiplexer U48, the bits being latched by U49. The EL EPROM U43 contains twice as many color tables as U44, as the EL display only requires two pixels for driving in each case.

The complex EL interface in U54 (ELINTER, EP910-30) includes a 4:1 multiplexer which is controlled by bits 3 and 4 in the ELREG control register U8.

The synchronization and clock signals for the EL display and CRT monitor are switched with U46 (PAL). U46 basically takes care of switching the processors to the various displays. The output signals to the EL display are latched via U2 to achieve synchronization between the SYNC signals, the EL clock and the pixel data for the EL display.

9.5.5 Keyboard (20) [2101-AJ]

There are three function blocks on the keyboard board.

Front panel LED controller

The LED controller is formed by two 8-bit latches (IC3,IC4) connected to the keyboard controller data bus. The latches accept data on the rising edges of control signals "CSW_LED_P1" and CSW_LED_P2".

Key matrix

The rows are driven sequentially with a LOW signal from the 1 from 8 decoder (IC2) (CS_ROWxy) and the columns read each time via IC1 (CSR_INT_DATA = LOW) from the keyboard controller.

STANDBY key and ON/OFF-LED

(see "Standby function" on page 9-37)

9.5.6 Rotary control (21) [2101 AK]

The rotary control board requires three operating voltages +5 V, +12 V and -12 V which are fed to the board via ST4. Of the 4 function blocks, three evaluate the rotary sensor and one handles the probe operating voltage:

- Control and evaluation logic
- Continuous operation
- Locked operation

The probe power supply is not fitted when this board is used in the SNA as no probes are used.

Initialization

The keyboard controller initialization routine sets the following states on the rotary control when the instrument is switched on:

- "RAST" = HIGH ==> continuous operation
- SPERR_DREHKNOPF" = HIGH ==> rotary control active
- 16-bit counter is set to 8000 Hex
- The counter high byte is read out to enable the clock

Communication to the keyboard controller

The interface to the keyboard controller is formed by the 8-bit data bus, via which the counter values are read or the counter is set, and to which one read and one write port are connected. IC15, IC16 IC23 and IC24 make up the counter. The write port (latch, IC18) is written to using the active-low control signal "CSW_STAT_DREHK". IC17 serves as the read port, which is read with the active-low signal "CSR_DREHKNOPF". The keyboard controller polls the read port. If the signal "DREHKNOPF" (IC7, PIN 13) is HIGH during the read operation, the rotary control was moved and the counter value is read out and then reset to 8000Hex. The rotary control is disabled during read, to ensure that the counter value does not change between reading the high byte and the low byte. The rotary control is then reactivated by the active-low signal "CSW_RES_DREHK".
The rotary control can be disabled, i.e. the signal "DREHKNOPF" is blanked, by setting the signal "SPERR_DREHK" at the write port to LOW.

Continuous operation

In continuous operation, the signal "RAST" is HIGH. The inverted RAST signal is used to enable the clock generator monostable (IC6.1) via IC3 and IC4.2. The rotary sensor B1 operates as a generator in continuous operation.

Rotary control idle state

The motor does not supply voltage and the capacitors C11, C12, C51, C53, C35 are discharged. TP1 is at +2.5 V, the D input of IC3.2 is at +5 V and the D input of IC3.1 is at 0 V. The outputs of IC3 assume the following values with the clock generated by IC7.4, R34 and C34:

IC3.1 Q = HIGH
IC3.2 Q = LOW

These signals reset the monostable IC6.1 via IC4.2 and thus hold the clock for the 16-bit counter to HIGH via IC8.2 and IC7.2.
The signal "DREHKNOPF" is set to LOW via IC8.3 and IC11.2; this signals to the keyboard controller that the rotary control was not moved.

Rotary control clockwise rotation

The rotary sensor generates a negative voltage when turned clockwise. If the voltage level is below -1.4 V (rapid turning), the capacitors C11, C12, C51, C53 and C35 are negatively charged via R3 or via R11 if the control is turned slowly. The counter value changes in proportion to the rotation speed if the capacitors are charged via R11, or over-proportionally when they are charged via R3 (rapid rotation). The negative voltage on the capacitors is amplified by IC9. TP1 is then at 0 V. The D input of IC3.2 is LOW which enables the clock generator monostable (IC6.1) via IC4.2. The clock pulses cause the capacitors C11, C12, C51, C53 to discharge via IC1.2 and T1. The idle state is present at TP1again when the capacitors are discharged.

The direction of rotation is detected at the $\overline{Q}$ output of IC3.2 and passed on to the counter via IC4.3. The $\overline{Q}$ output of IC3.2 is HIGH for clockwise rotation, i.e. the counter increments starting from 8000Hex. Incrementing can only be halted by reading out the counter or disabling the clock.

Rotary control anticlockwise rotation

The rotary sensor generates a positive voltage when turned anticlockwise. The voltage polarity generates the direction of rotation signal at the $\overline{Q}$ output of IC3.2. The $\overline{Q}$ output is set LOW for anticlockwise turing, i.e. the counter decrements starting from 8000Hex. The remaining function is as for clockwise operation.

Locked operation

The signal "RAST" is LOW for locked operation, as the rotary sensor is not used as a generator but as a motor. The rotary sensor is the control element in a control loop. The arrangement of reflected light barriers and the voltage gain for controlling the motor simulate the 16 stable changeover switching points of a mechanical switch. An additional audible "click" (LSP1 and IC.7.6) enhances the effect of a mechanical switch each time changeover occurs.

Rotary control idle state

The rotary sensor is held at a stable locking point, i.e. the motor voltage is 0 V. The counter does not receive clock pulses and stays set to 8000H.

Clock and direction signal for 16-bit counter

The comparators IC14 and IC21 amplify the signals from the reflected light barriers to TTL level. The reflected light barriers generate different phase-shifted pulses, depending on the direction of rotation. Turned clockwise, EK3 lags 90 degrees behind EK2 and EK1 is 180 degrees out of phase with EK2.
Turned anticlockwise, EK3 leads EK2 by 90 degrees and EK1 is 180 degrees out of phase with EK2.
IC19.1 generates a 190 s pulse on the negative edge of EK2 and IC19.2 on the positive edge. IC4.4 blanks out the pulses on the positive edge during clockwise rotation and the pulses on the negative edge during anticlockwise rotation. The output signal from IC4.4 is passed to the counter (IC16, IC15, IC23, IC24) via an enable gate.
The direction of the counter is derived directly from EK2. This is HIGH on the positive clock edge of the 16-bit counter for clockwise rotation and LOW for anticlockwise rotation.

Motor controller

When the rotary sensor is turned a voltage is induced which opposes the rotation until the voltage at EK2 is reversed, i.e. the reflected light barrier changes its logical level and the rotary control pulls itself to the next stable state.

9.5.7 Keyboard controller (19) [2101-AL]

The keyboard controller is IBM-MF2 compatible. It uses the German character set (if KEYBYY=GR in the file B:\Auto2.bat of the SNA is selected).
An external MF2 keyboard (AT keyboard) can also be connected to the controller. Both keyboards (internal instrument keyboard and external keyboard) can then be used simultaneously.
The keyboard controller is made up from the following function groups:

- Processor core
- Interface to AT CPU (SIM386)
- Internal keyboard driver
- External keyboard driver
- Rotary control driver

The initial delay (500 ms) and the repetition rate (10 Hz) are fixed for the internal keyboard. The external keyboard can be set as desired from the AT CPU (from the AT CPU setup).
The electrical signals on the interface have TTL level.

Processor core

The microcontroller 80C39 is clocked with 10 MHz. The RESET of the 80C39 is linked to the instrument reset.

P10 to P13	serve for communication with the AT CPU
P14 to P16	serve for communication with the external keyboard.
P20 to P23	are the address lines A8 to A11 during read operations from EPROM and otherwise are four I/O circuits.

Interface to AT CPU (SIM386)

The data traffic between the keyboard and the AT CPU is via the circuits "AT_KEY_CLK" and "AT_KEY_DATA". Each data word comprises 1 start bit (LOW), 8 data bits, 1 parity bit and 1 stop bit (HIGH).

Interface to internal keyboard

P24 to P27 are fed to the keyboard board. They control the 16 rows of the key matrix. The row information for the keys is read with signal "CSR_INT_DATA".
When P13 is LOW, the processor detects that the AT CPU has data to transmit.
Among other things, the EPROM (IC3) contains a table of key codes to be transmitted when a key is pressed. Since the processor can only drive a maximum of 4Kb EPROM, the jumpers ST2, ST3 and ST4 are used to select one of eight pages in the 32Kb EPROM. Page 0 (no jumpers set) contains the program with the KEYBOARD conforming codes for the internal keys. Page 1 (jumper ST4 set) contains the key number conforming codes for the internal keys.
The LEDs on the internal keyboard are driven by two latches on the keyboard (20IC3 and 20IC4) which are driven by the signals LED_1 and LED_2.

Interface to external keyboard

When the external keyboard is operated, the keyboard scan codes are transmitted unchanged to the AT.
The codes from the external keyboard are inverted and read into shift register IC11 or IC12 by the signals "EXT_KEY_CLK" and "EXT_KEY_DATA". Once all the bits have been received by the shift register, output IC11/5 is HIGH. This signal disables the external keyboard for further transmission via the open collector driver IC14.5. The same signal is continuously polled by the processor via circuit T0, the processor thus detects that the external keyboard has transmitted

a character. The characters from the external keyboard are read in via ports IC9 and IC10 and put in the stack before being transmitted to the AT-CPU. After reading the external characters, the shift register is reset with "CSW:RESET".
Commands to the external keyboard are transmitted using the same protocol as is used by the AT CPU to the internal keyboard controller. This communication is via ports P14 to P16.

Rotary control driver

The keyboard controller initialization routine sets the following states on the rotary control:

- "RAST" = HIGH ==> continuous operation
- SPERR_DREHKNOPF" = HIGH ==> rotary control active
- 16-bit counter is set to 8000 Hex
- The counter high byte is read out to enable the clock

The controller software monitors the rotary control by polling the read port (21IC17) on the rotary control board which is activated by the control line "CSR_DREHKNOPF" = LOW. If the pulse generator is moved, D(1) = HIGH.
"CSR_DREHZAEHLER_LOW" and "CSR_DREZAEHLER_HIGH" are used to read out the 16-bit counter on the rotary control board (both signals active-low).
The write port (21IC18) on the rotary control is written to on the positive edge of the signal "CSW_STAT_DREHK". The contents of the write port sets whether the rotary control is active or disabled. The port also includes the information whether the rotary control was locked or continuously operated.

Lock on	==> D(0) = LOW
Lock off	==> D(0) = HIGH
Rotary control active	==> D(1) = HIGH
Rotary control disabled	==> D(1) = LOW

The signal "CSW_RES_DREHK" (dynamic, active-low) enables the rotary control after initialization.

9.6 Power supply unit

The SNA uses the AC PSU CG 44 manufactured by Gossen. This AC PSU supplies the following voltages and control signals to sockets BUX1 and BUX2:

BUX1	BUX2
+5 V	TOO HOT
+23 V	SAVE DATA
+6,8 V	SYNSIG
-6,5 V	-21 V
+18 V	+12 V
+12 V	FAN
-12 V	STDBY

Table 9-2 Output voltages and control signals from the AC PSU

9.6.1 Voltage distribution (1) [2101-BD]

The module-specific supply voltages are fed to the voltage distribution board (1) [2101-BD] from the AC PSU (plug X1) and then to the individual modules.

Plug 4 ===> 16 J16 interface board (CPU, memory, BSK-3)
Plug 5 ===> Floppy (AT-CPU)
Plug 6 ===> 3 P10 controller YIG filter
Plug 7 ===> 5 ST8 controller input section
Plug 8 ===> 50 ST13 Timebase/YTO driver (synthesizer)
Plug 9 ===> 12 ST10 IF distortion (radio link), not used in SNA
Plug 10 ===> 11 ST1 calibration generator, demodulator, IF measurement unit
Plug 16 ===> Tracking generator (instrument back panel)

A further plug (X2) from the AC PSU carries two auxiliary voltages, -21 V and +12 V, the AC PSU fan connection and the following data circuits for plug ST1 on the voltage distribution board:

- TOO HOT
- SAVE DATA
- SYNCHRONIZATION
- STANDBY

The instrument fan is connected to plug ST 3 on the voltage distribution board. The speed of the fan is controlled between 30°C and 50°C by connecting a NTC thermistor to ST14. If ST14 is shorted out (standard for SNA), the fan runs at full speed. Comparator IC5.2 switches the fan on at 10 °C.

Plug ST 2 connects the standby key and the standby LED to the controller.

The following voltages are available via the connection from plug ST12 to socket BU15 on the back panel:
From voltage regulators IC9 and IC10: +5 V/0.5 A; +15 V/0.35 A. Also, -12 V/0.1 A at Ri = 10 Ω is available. The two voltage regulators IC9 and IC10 operate without heatsinks to ensure that they switch off thermally when the current load is too high. The -12 V supply is fed to ST 12 via a 6.04 Ω resistor. The voltage source thus has a source impedance of about 10 Ω.

Standby function

With AC power "on" and "standby" selected, all supply voltages except the +12 V auxiliary voltage are switched off, the standby LED is on and the AC PSU and instrument fans are off. Retriggerable monostable IC8.1 debounces the standby key. The monostable hold time is about 2.5 seconds. This pulse drives bistable relay Rel1 which is used as a notching relay with the adapter module IC4.

Synchronization signal

A 50 Hz sinewave signal is fed from the AC PSU ST X2 to voltage distribution board ST1.3. This is converted to a 50 Hz square wave by OP IC5.1 and connected to ST10.15 on the voltage distribution board. This signal (SYN50HZ) is fed to the IF measurement section (calibration generator) (11) ST1.

Save data

This signal is supplied directly to ST X2.2 by the AC PSU and is connected to ST1.2 on the voltage distribution board, from where it is taken via (1)ST4.2 to the interface board (16) on plug (16)ST16.

Too hot

The "too hot" signal can be generated by the AC PSU (overtemperature) and switches the to standby mode (LED = flashing) if overheating occurs. The signal can also be generated by temperature monitor IC5.3. This OP is set to about 4.3 V on pin 9 using potentiometer P1, which corresponds to a cutoff (standby) temperature of 55 °C. The "too hot" signal is fed via (1)ST4.3 to the interface board (16)ST16 where it is evaluated by the controller.

Too cold

"Too cold" is generated by temperature monitor IC5.4. If the temperature inside the instrument at sensor NTC R40 is below 0 °C, the "too cold" signal is HIGH. This signal is fed via (1)ST 4.1 to the interface board (16)ST16 where it is evaluated by the controller (LED = flashing).

9.6.2 24/12 V switching regulator

The switching regulator provides the supply voltage for the EL display. The regulator supplies 2.0 A at 12 V and a switching frequency of approx. 100 kHz, is fitted with 'soft start' and internal current limit functions.

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